Practical proof systems: Implementations, applications, and next steps

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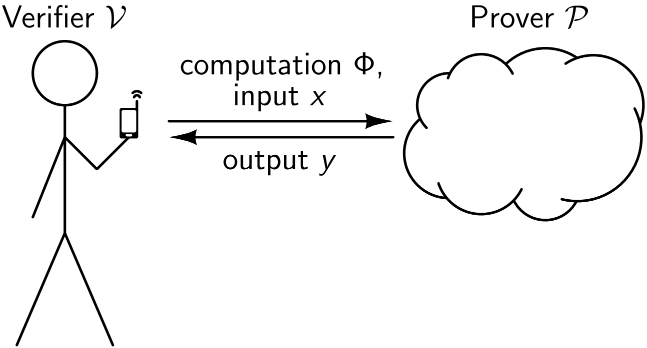
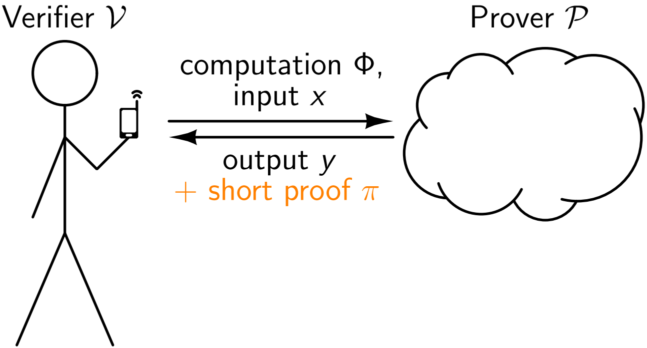
Stanford

September 23rd, 2019


Verifier $\mathcal{V}$
Prover $\mathcal{P}$
computation Φ,
input x
output y



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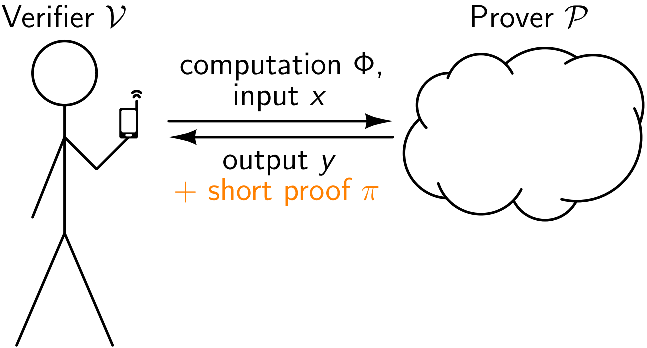

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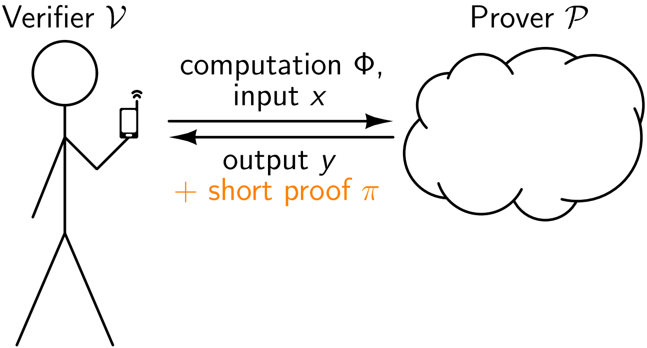

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SBW11
CMT12
SMBW12
SVPBBW12
TRMP12
BCGTV13
BFRSBW13
BFR13
DFKP13
PGHR13
SBVBPW13
VSBW13
BCGGMTV14
BCTV14a
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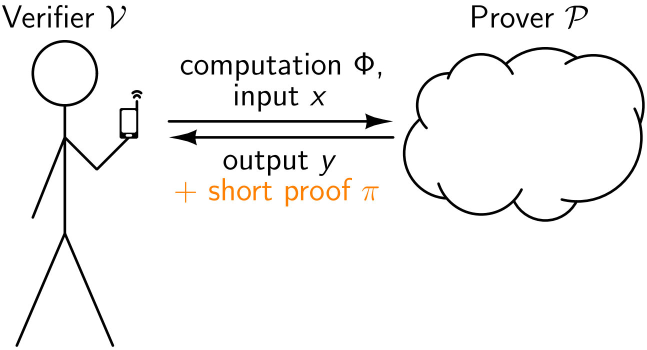
FL14
KPPSST14



BBFR15
CFHKKNPZ15
CTV15
KZMQCPPsS15
WSRHBW15
D-LFKP16
FFGKOP16
GMO16
NT16
WHGsW16
AHIV17
CDGORRSZ17
WJBsTWW17
ZGKPP17a
ZGKPP17b
BBBPWM18
KPS18
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Bottom line: this is a huge tradeoff space!

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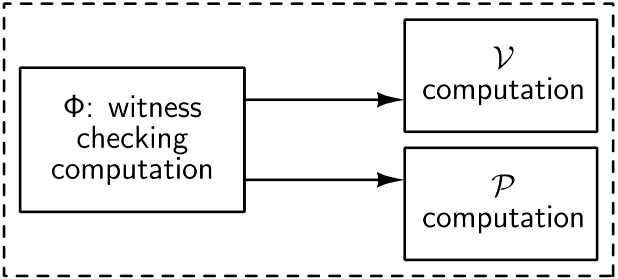

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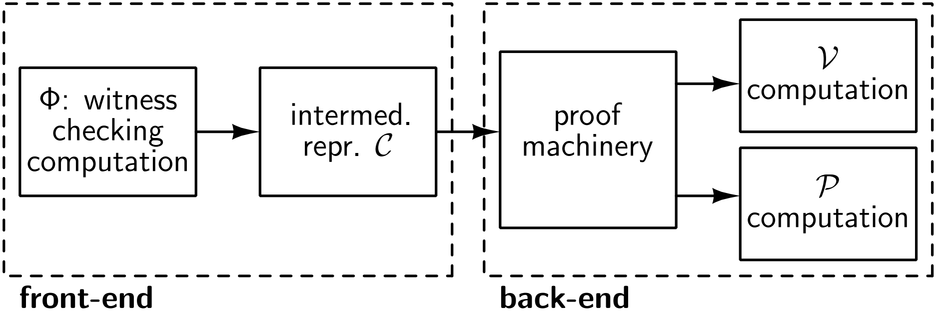

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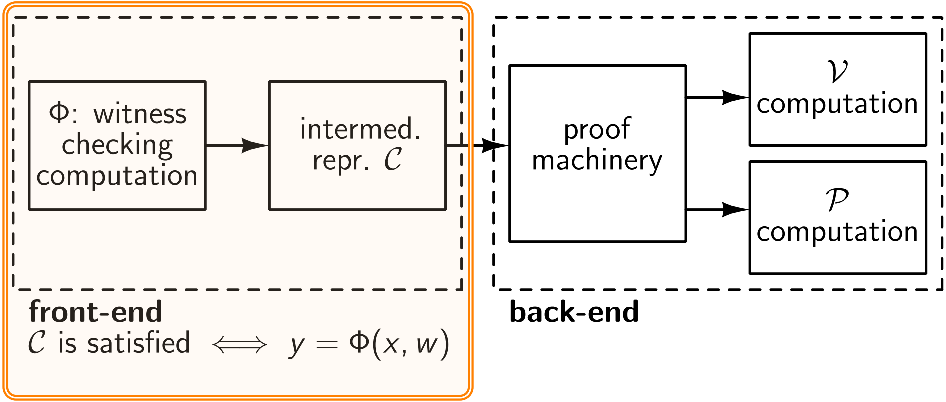

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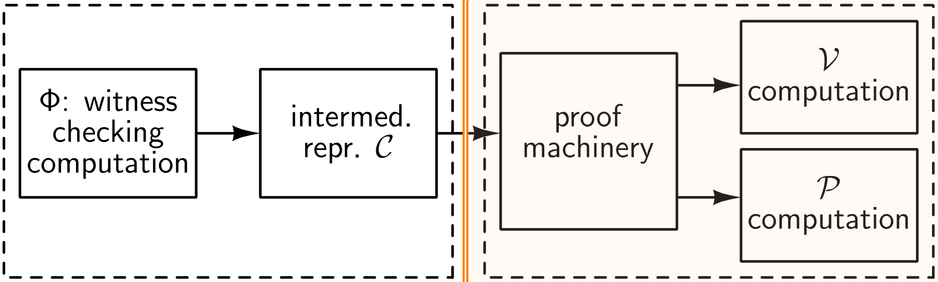

front-end
$\mathcal{C}$ is satisfied $\iff$ $y = \Phi(x, w)$

back-end
valid proof $\iff$ $\mathcal{C}$ is satisfied

Underlying machinery

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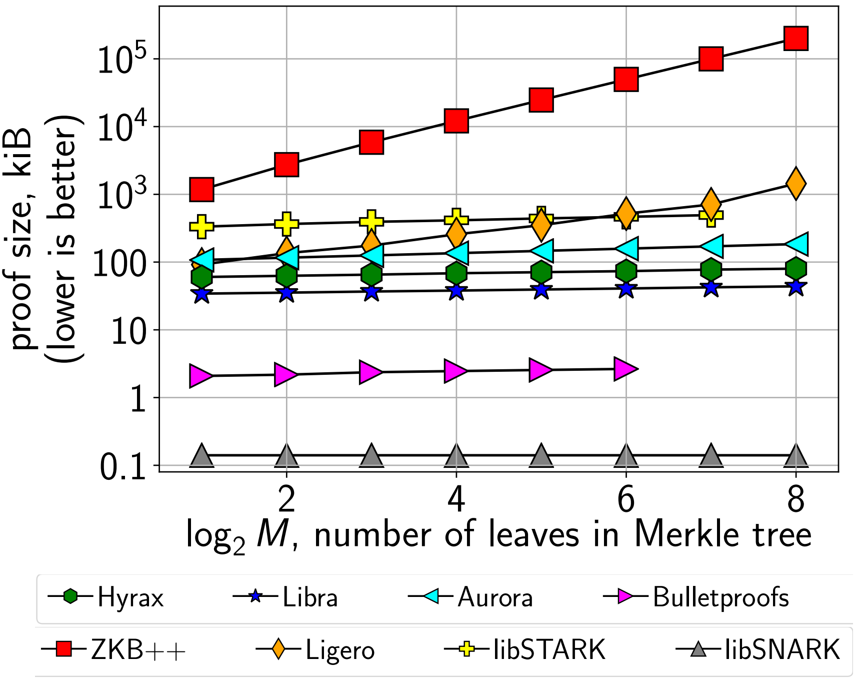

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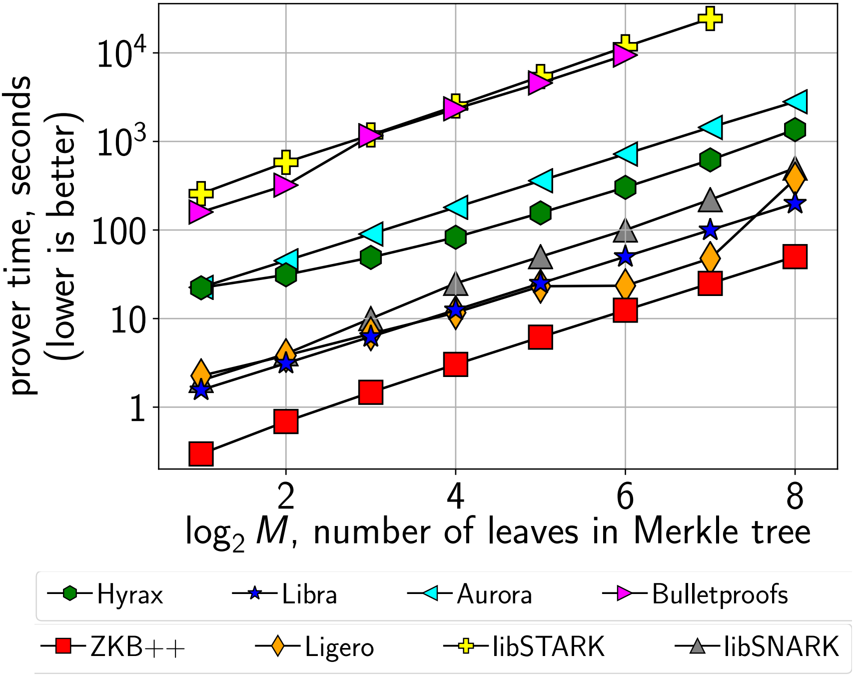

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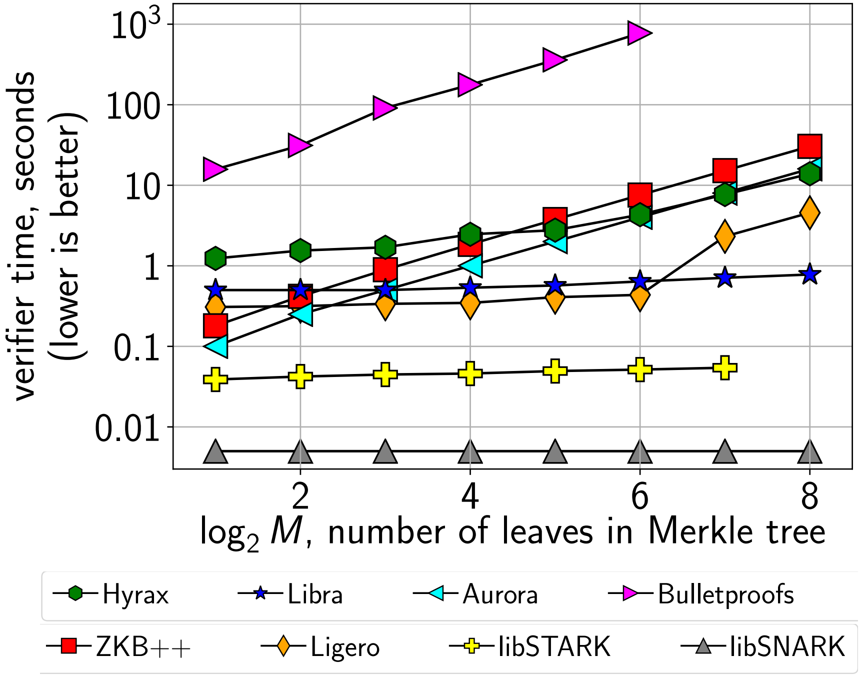

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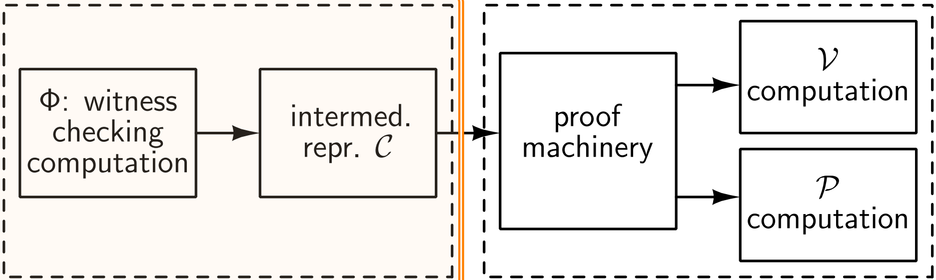
Proof system construction

On input x, $\mathcal{P}$ convinces $\mathcal{V}$ that $y = \Phi(x, w)$
for a witness w that $\mathcal{P}$ knows



front-end
$\mathcal{C}$ is satisfied $\iff y = \Phi(x, w)$

back-end
valid proof $\iff \mathcal{C}$ is satisfied

Representing Φ for execution on the back-end

"CPU": run Φ on unrolled FSM

fetch-decode-execute step 1	fetch-decode-execute step 2	. . .	fetch-decode-execute step T
CPU state: pc, regs, . . .	CPU state: pc, regs, . . .		CPU state: pc, regs, . . .

[BCGTV13,BCTV14a,BCTV14b,CTV15,ZGKPP18,BBHR19]

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“FPGA”: translate Φ directly to AC or constraints

```
if (i >= 5)
    i = i + 1;
else
    i = i * 2;
```

$\Longrightarrow$

```
i1 = i0 + 1;
i2 = i0 * 2;
i3 = (i0 >= 5) ?
        i1 : i2;
```

[. . . , SVPBBW12, BFRSBW13, SBVBPW13, PGHR13, VSBW13, BBFR15, CFHKKNPZ15, KZMQCPPsS15, WSRHBW15, BCCGP16, BBBPWM18, KPS18, BCRSVW19, MBKM19, Circom, Bellman, . . .]

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[CMT12, WHGsW16, WJBsTWW17, WTsTW18, XZZPS19]

Representing Φ for execution on the back-end

"CPU": run Φ on unrolled FSM

```
// assume i0 is k+1 bits
i4 = i0 - 5;
// prover supplies i4_0, ..., i4_k
assert (i4 - i4_0 - 2 * i4_1 - ... - 2^k * i4_k == 0);
assert (i4_0 * (1 - i4_0) == 0);
...
assert (i4_{k-1} * (1 - i4_{k-1}) == 0);
assert (i4_k == 0);
```

nts

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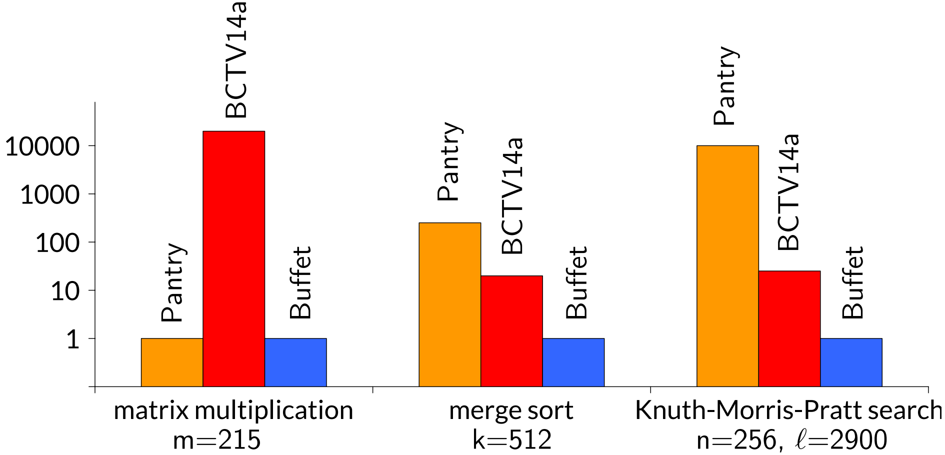
Performance vs. expressiveness

costs	special purpose	pure	stateful	general control flow
lower	[Tha13] vSQL [ZGKPP17] Bellman gadgetlib [BCTV14a] LegoSNARK [CFQ19] c0c0 [KZMQCPPsS15]	Giraffe [WJBsTWW17] Allspice [VSBW13] Zaatar [SBVBPW13] Pinocchio [PGHR13] Circom Ginger [SVPBBW12] Pepper [SMBW12]	xJsnark [KPS18] Geppetto [CFHKKNPZ15] ADSNARK [BBFR15] Pantry [BFRSBW13]	vRAM [ZGKPP18] Buffet [WSRHBW15] STARK [BBHR19]
				(vn)TinyRAM [BCTV14a] [BCGTV13]
higher				[BCTV14b] [CTV15]

better

Front-end comparison

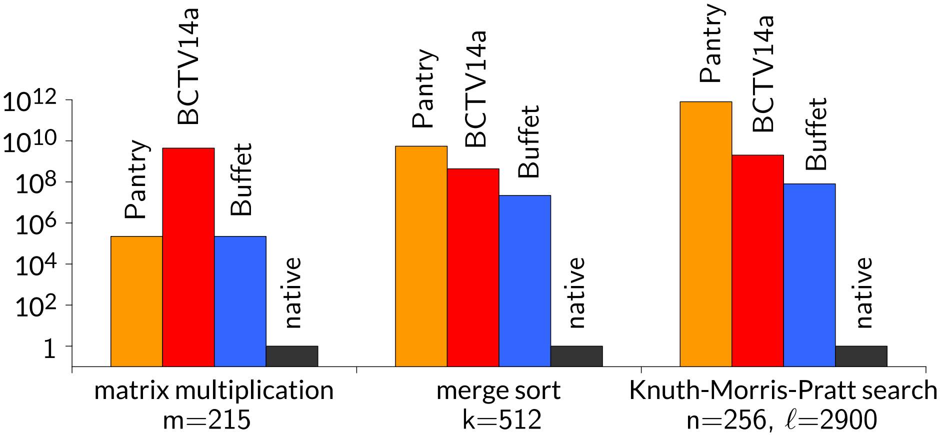
Extrapolated $\mathcal{P}$ execution time, normalized to Buffet



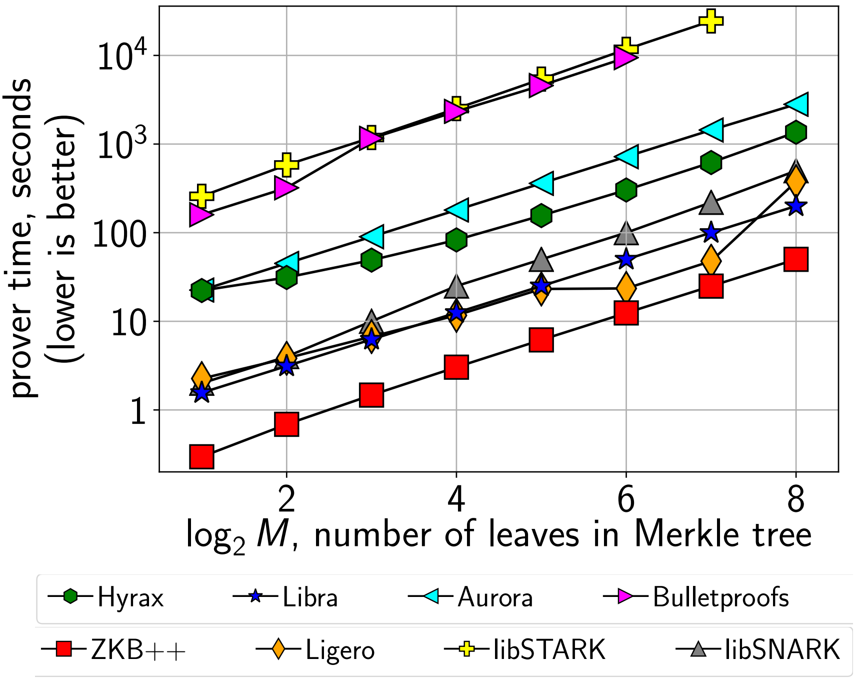
- xJsnark [KPS18] improves upon Buffet by up to ≈3×
- vRAM [ZGKPP18] (builds on and refines [Tha13] back-end) is ≈22× faster than Buffet for matmult, comparable otherwise

Reality check

Extrapolated $\mathcal{P}$ execution time, normalized to native execution



- xJsnark [KPS18] improves upon Buffet by up to $\approx 3\times$
- vRAM [ZGKPP18] (builds on and refines [Tha13] back-end) is $\approx 22\times$ faster than Buffet for matmult, comparable otherwise



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Reality check 2: reachable problem sizes

For $\approx 10^7$ gates, $\mathcal{P}$ needs $\approx$16–32 GiB of RAM.

Limiting computations to these sizes yields:

	Pantry	**BCTV14a**	**Buffet**
matrix multiplication $m \times m$	215	7	215
merge sort k elements	8	32	512
Knuth-Morris-Pratt search needle length $= n$ haystack length $= \ell$	$n = 4$, $\ell = 8$	$n = 16$, $\ell = 160$	$n = 256$, $\ell = 2900$

☞ vRAM [ZGKPP18] increases reachable sizes by $\approx 10\times$

DIZK [WZCPS18]: distributing $\mathcal{P}$'s workload

Idea: run $\mathcal{P}$ as a distributed computation

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(among others)

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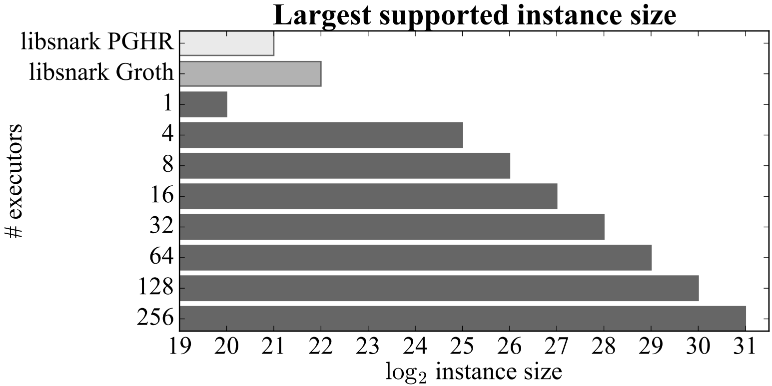
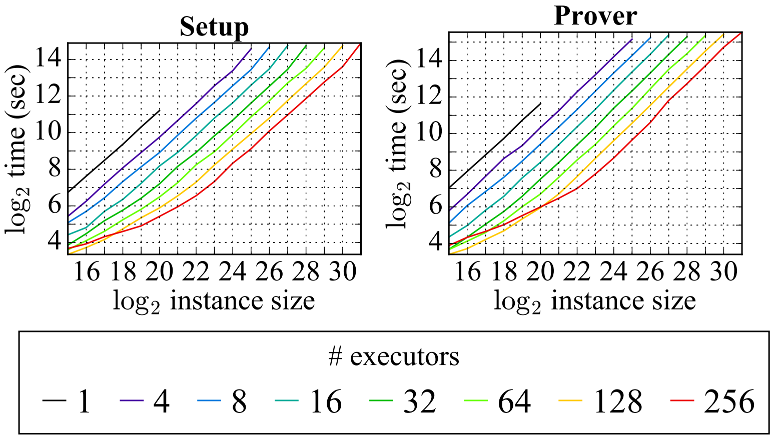
☞[Sze11]: converts size-n FFT to two $\sqrt{n}$-sized batches of $\sqrt{n}$-sized tasks

DIZK: 100× larger instances



[WZCPS18, Fig. 4]

DIZK: 100× faster execution



[WZCPS18, Fig. 5]

Cryptocurrencies!

ZCash (following [BCGGMTV14]) uses ZK for

- anonymity: no one knows who you are
- privacy: transaction values are hidden

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☞ constant-sized blockchain via recursive proof composition

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☞ constant-sized blockchain via recursive proof composition

Private airdrops [BJPW19] (ePrint soon)

free money from the internet using existing credentials (e.g., GitHub) without revealing your identity

☞ *not* a general-purpose proof system!

Let's build a bank out of a smart contract!

Roll_up

https://github.com/barryWhiteHat/roll_up

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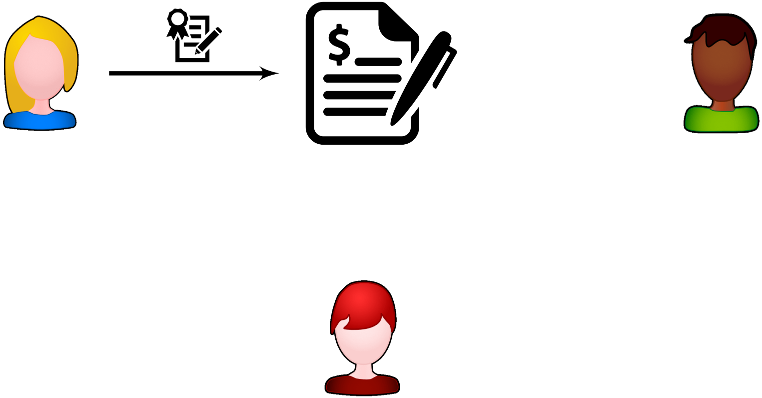

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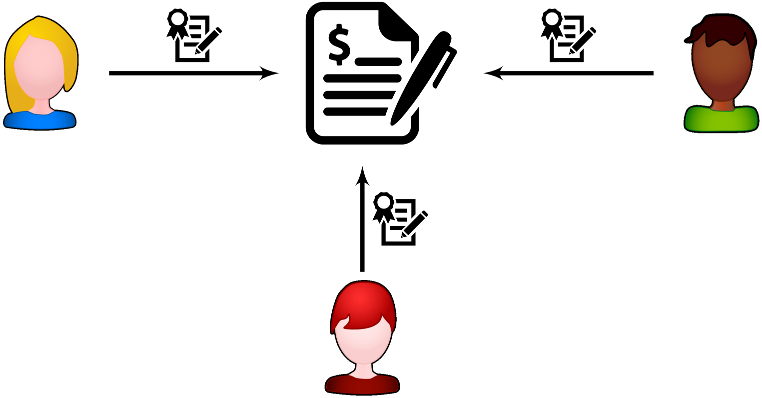

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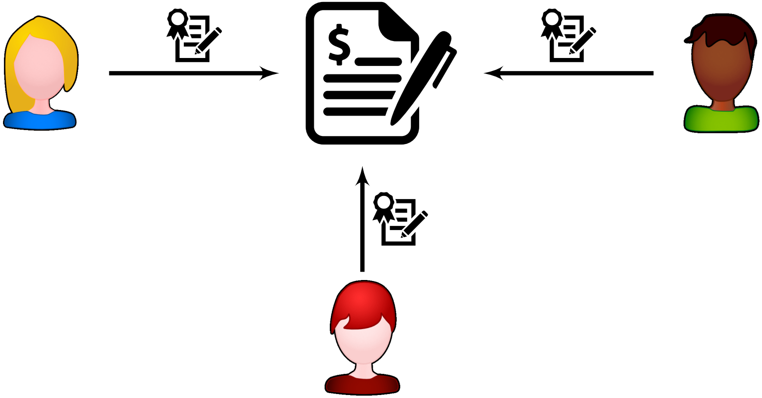

Issues: on-chain work and data cost $$$!; slow!

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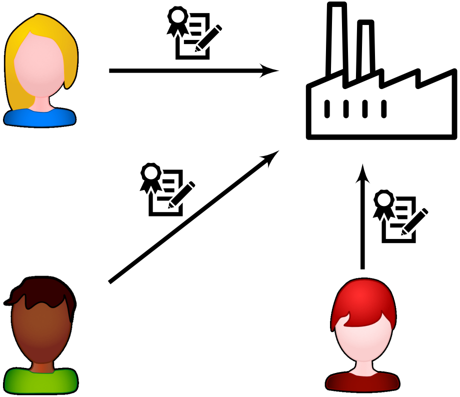

Idea: use an off-chain, *untrusted* aggregator

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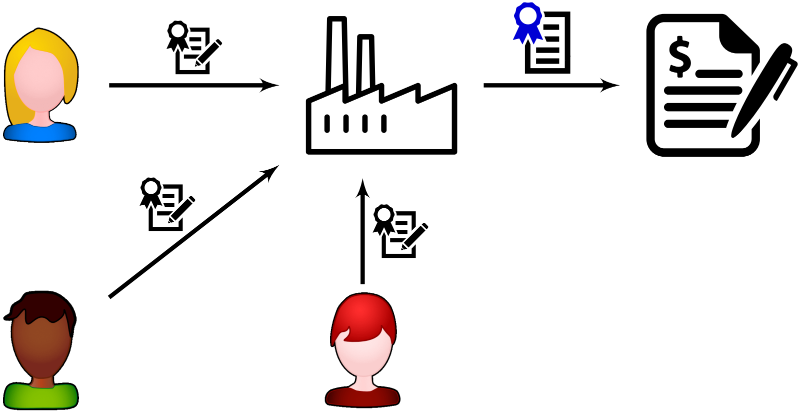
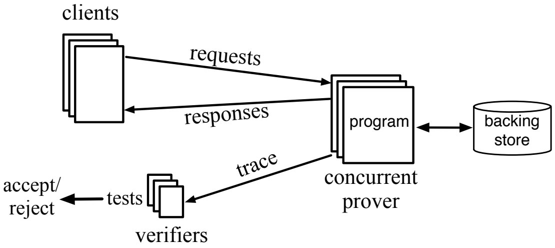


Idea: use an off-chain, *untrusted* aggregator to prove validity of a batch of transactions

Spice [SAGL18]: verifiable *concurrent* services (in ZK)

(e.g., a cloud-hosted wallet service.)



[SAGL18, Fig. 1]

Issue: need verifiable storage with concurrency

Spice [SAGL18]: verifiable *concurrent* services (in ZK)

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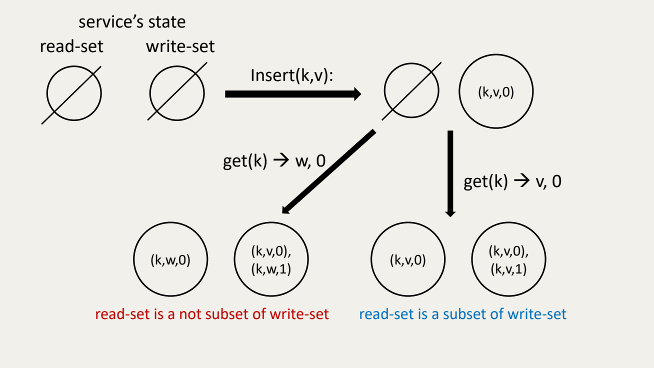
Idea: adapt primitives from memory checking literature [BEGKN91,CDDGE03,AEKKMPR17]



(source: Srinath's talk)

Spice [SAGL18]: verifiable *concurrent* services (in ZK)

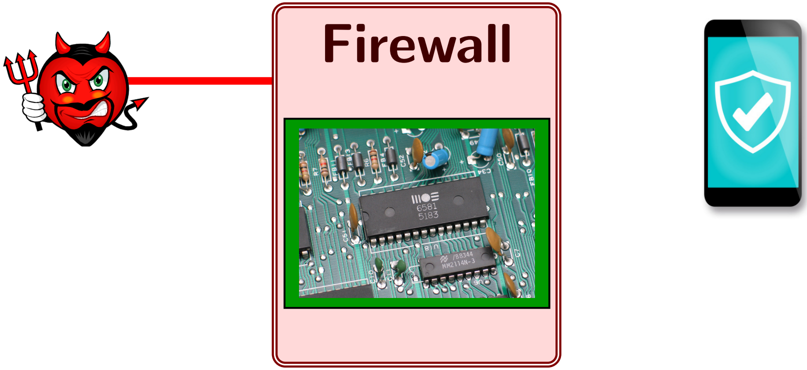
(e.g., a cloud-hosted wallet service.)

Performance results:

	`get`	`put`
Pantry	0.078	0.039
Pantry+Jubjub	0.153	0.076
Geppetto	0.002	0.002
Spice (1-thread)	3.6	3.6
Spice (512-threads)	1366	1370

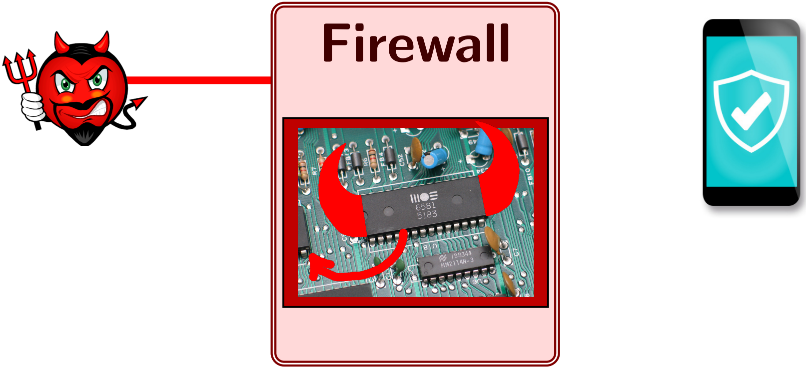
[SAGL18, Fig. 9]

How can we build trustworthy hardware?



e.g., a custom chip for network packet processing whose manufacture we outsource to a third party

Untrusted manufacturers can craft hardware Trojans



What if the chip's manufacturer inserts a **back door**?

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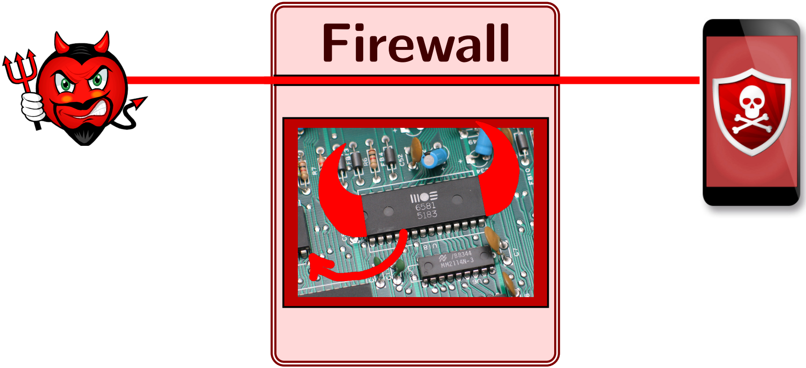

What if the chip's manufacturer inserts a **back door**?

Threat: incorrect execution of the packet filter

(Other concerns, e.g., secret state, are important but orthogonal)

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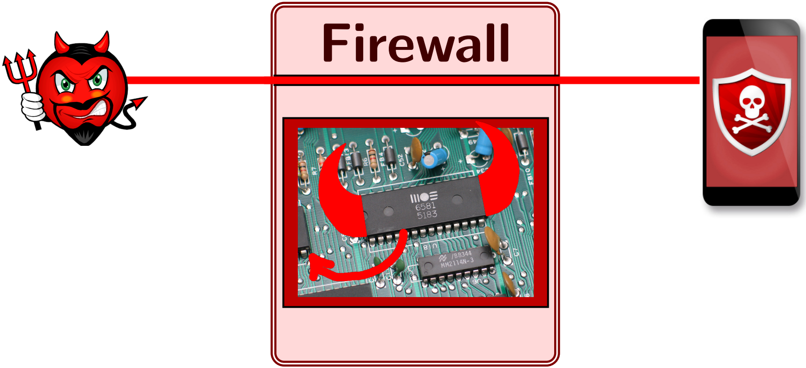

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The Cybercrime Economy

Fake tech gear has infiltrated the U.S. government

by David Goldman @DavidGoldmanCNN

November 8, 2012: 3:10 PM ET

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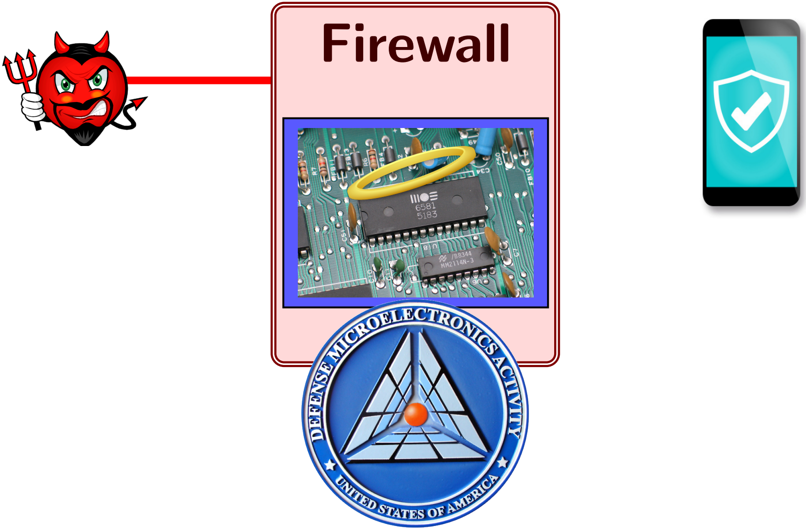

US DoD controls supply chain with **trusted foundries**.

Trusted fabs are the only way to get strong guarantees

For example, stealthy trojans can thwart post-fab detection
[A2: Analog Malicious Hardware, Yang et al., Oakland16; Stealthy Dopant-Level Trojans, Becker et al., CHES13]

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Idea: outsource computations to untrusted chips

Verifiable ASICs [WHGsW16,WJBsTWW17]

$\boxed{\begin{array}{c}\text{Principal}\\ \Phi \to \text{designs}\\ \text{for } \mathcal{P}, \mathcal{V}\end{array}}$

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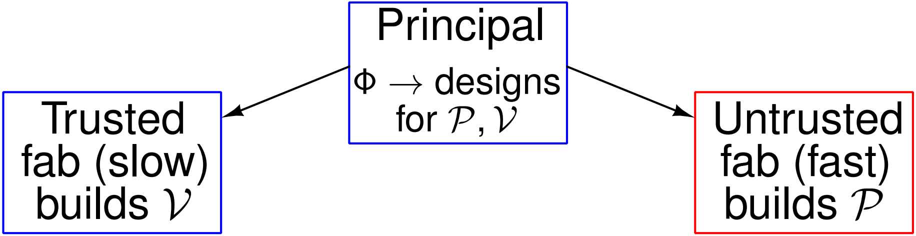

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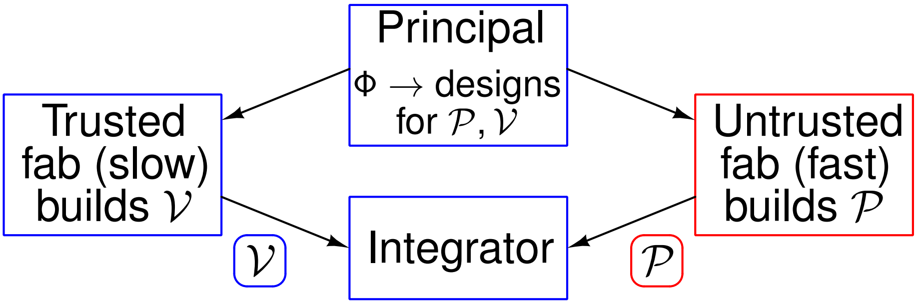

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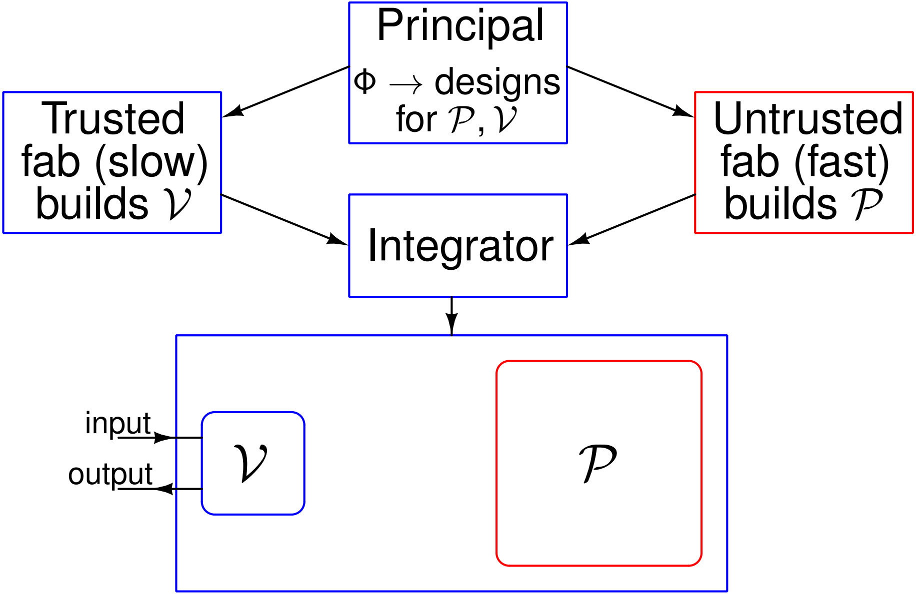

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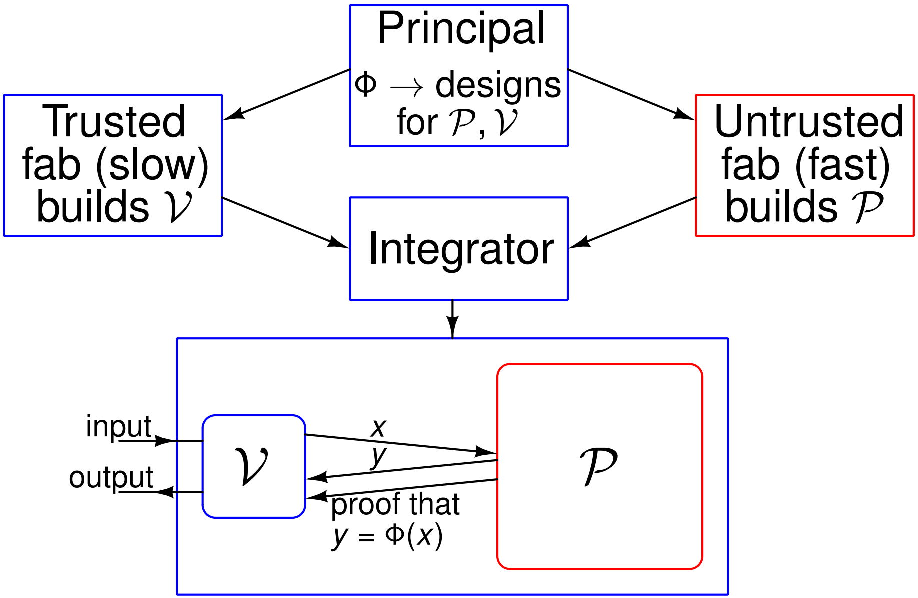
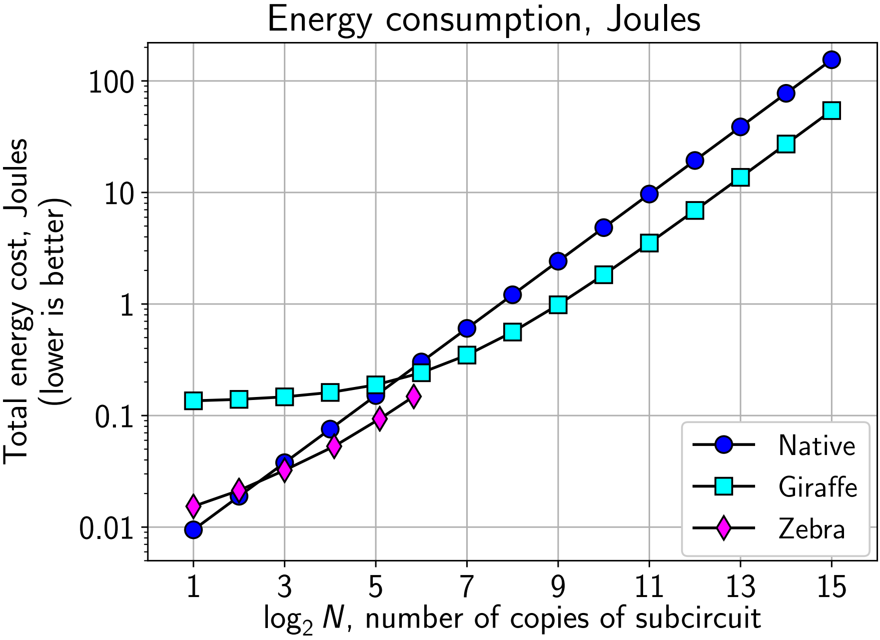


Verifiable ASICs [WHGsW16,WJBsTWW17]: Curve25519



Wishlist: back-ends

avoiding FFTs

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updateable SRS with updateable proofs

☞ some steps in this direction:
[Lip19] `https://ia.cr/2019/333`

Wishlist: front-ends

beyond the AC model

- ☞ "natural" computations are ugly as ACs: bitwise ops, comparisons; this is a *major* cost, e.g., in SHA-256 TinyRAM [BCGTV13,BCTV14a], vRAM [ZGKPP18], STARK [BBHR19] point the way; can we go further?

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compilers for everyone!

- ☞ recent work *hand tunes* statements, relies on authors' intuition and implicit knowledge
  let's *systematize* this knowledge, *automate* tuning
- ✓ improved accessibility and real-world deployability
- ✓ highly leveraged work for the research community:
  simpler, higher quality evaluations, easier-to-interpret results

Recap

- ☞ huge design space!

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…and plenty of research questions to explore!

`rsw@cs.stanford.edu`