Verifiable ASICs: trustworthy hardware with untrusted components

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Siddharth Garg[⋆], abhi shelat[‡], and Michael Walfish[⋆]

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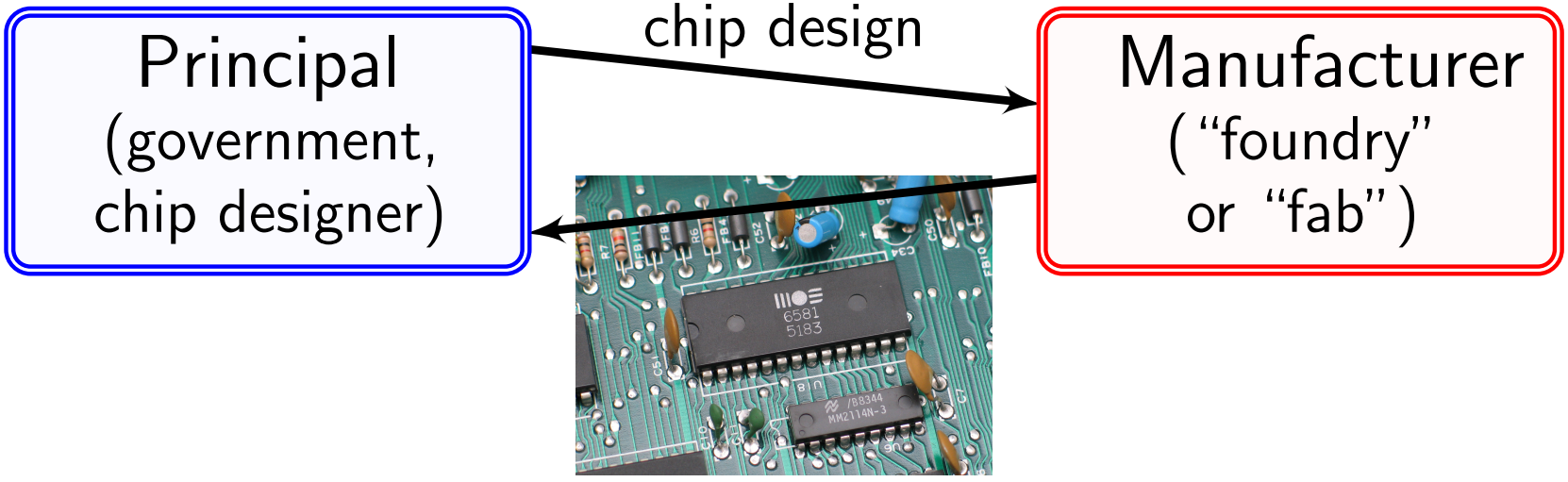
[⋆]New York University
[†]The Cooper Union
[‡]The University of Virginia

June 10th, 2016

Setting: ASICs with mutually distrusting designer, manufacturer



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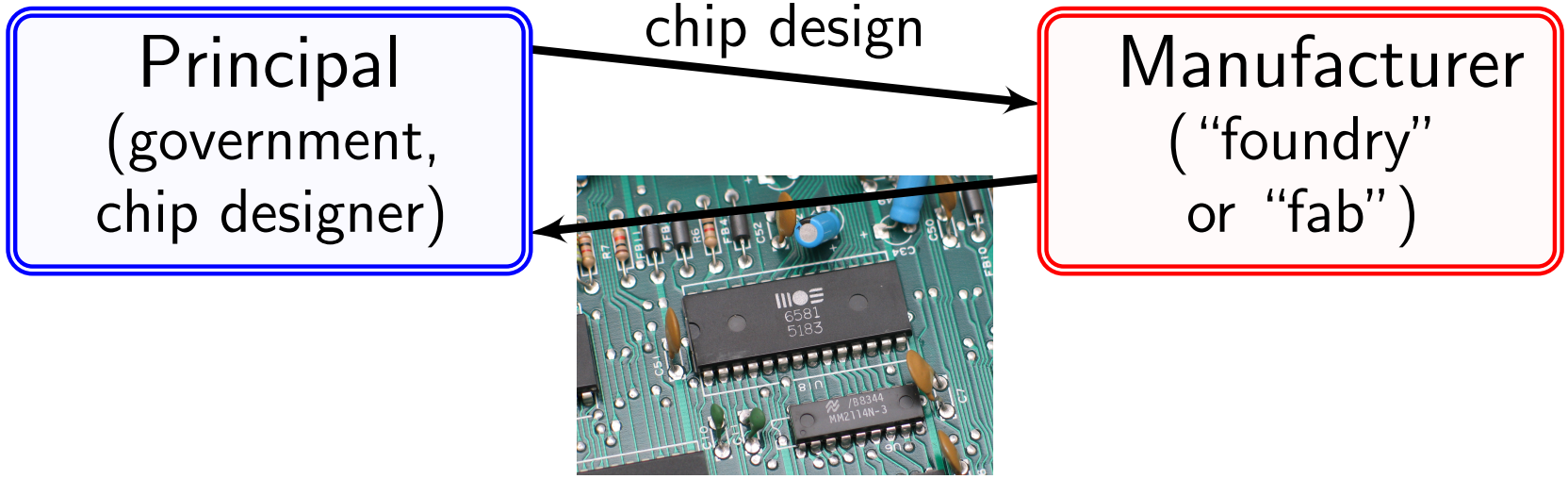
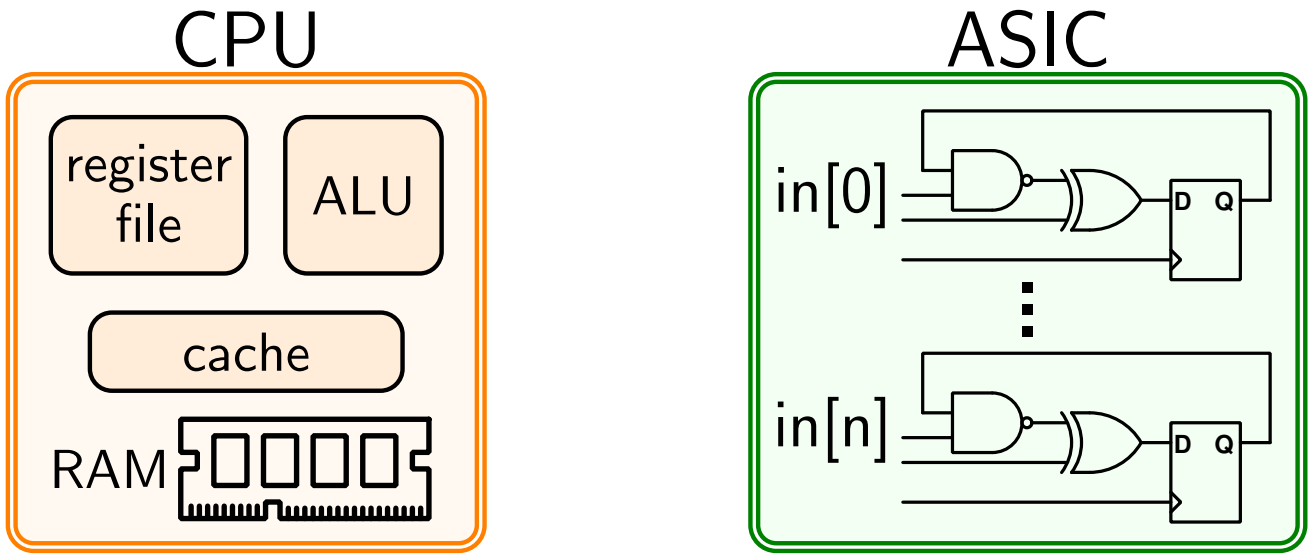


Here we are thinking about ASICs, not CPUs:



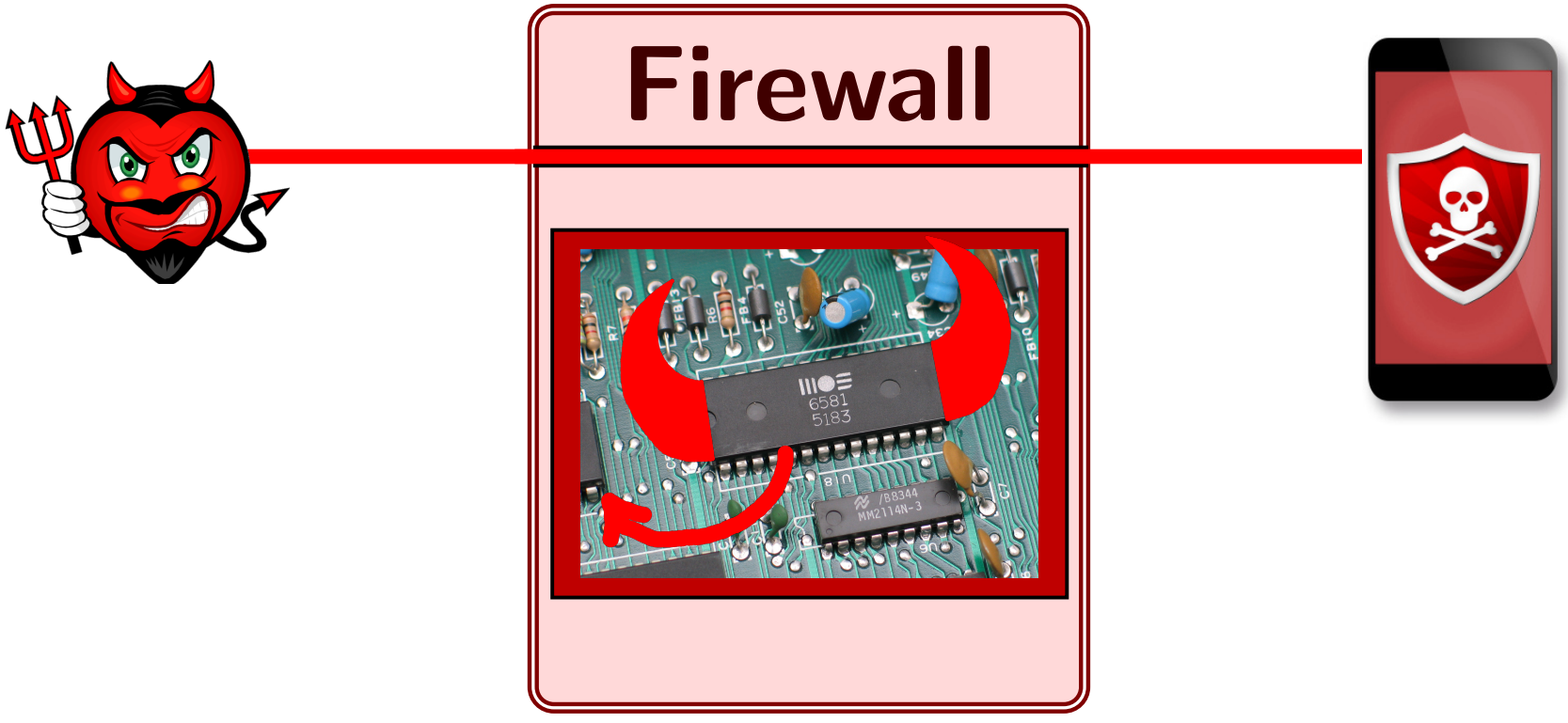
Setting: ASICs with mutually distrusting designer, manufacturer

e.g., a network firewall appliance,
with a custom chip for packet processing

Untrusted manufacturers can craft hardware Trojans

What if our packet processing chip has a **back door**?

Untrusted manufacturers can craft hardware Trojans



What if our packet processing chip has a **back door**?

Threat: incorrect execution of the packet filter

(Other concerns, e.g., secret state, are important but orthogonal)

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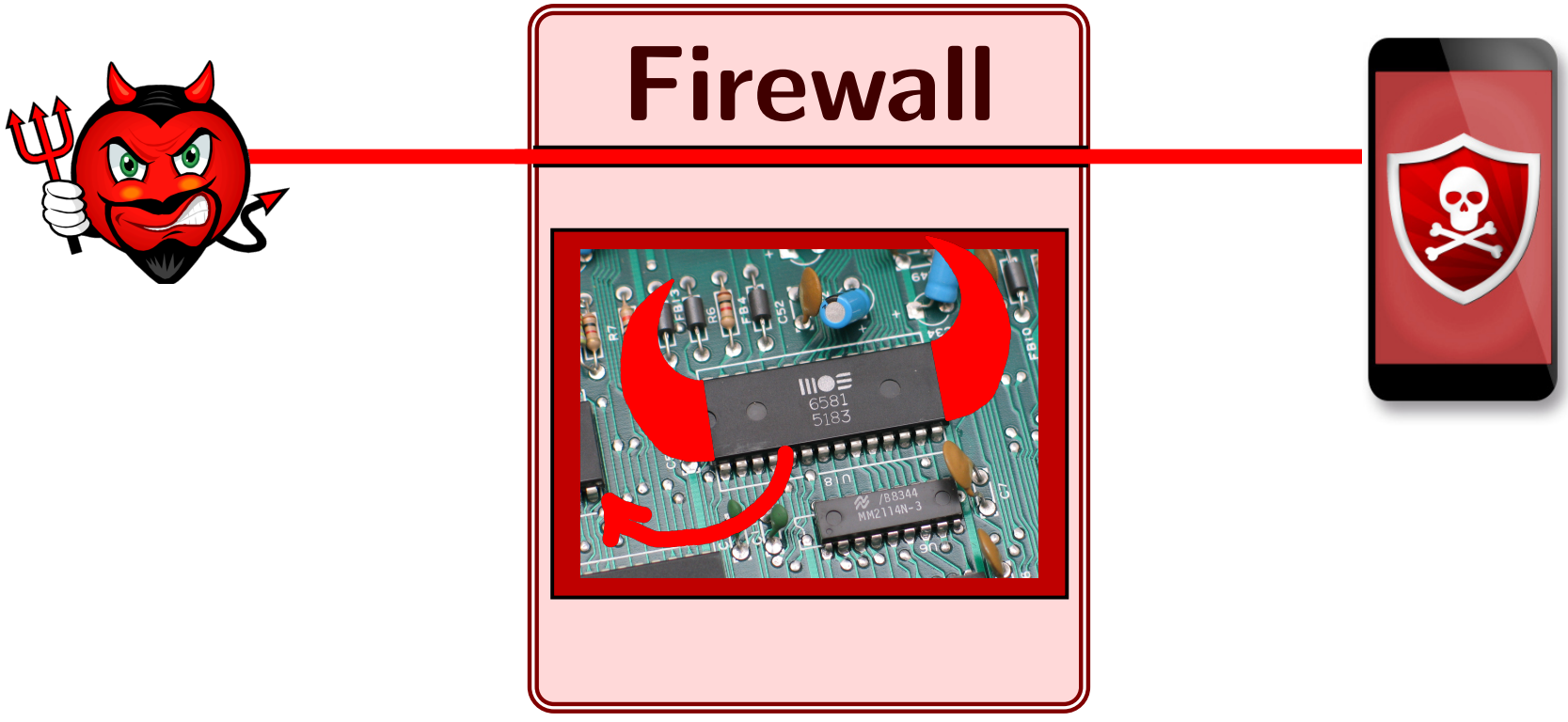


What if our packet processing chip has a **back door**?

The Cybercrime Economy

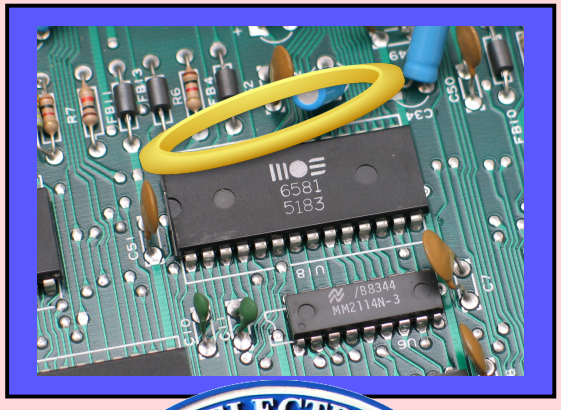
Fake tech gear has infiltrated the U.S. government

by David Goldman @DavidGoldmanCNN

November 8, 2012: 3:10 PM ET

Untrusted manufacturers can craft hardware Trojans

Firewall



US DoD controls supply chain with **trusted foundries**.

Trusted fabs are the only way to get strong guarantees

For example, stealthy trojans can thwart post-fab detection
[A2: Analog Malicious Hardware, Yang et al., IEEE S&P 2016;
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- ✗ Only 5 countries have cutting-edge fabs on-shore
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  e.g., India's best on-shore fab is $10^8\times$ behind state of the art

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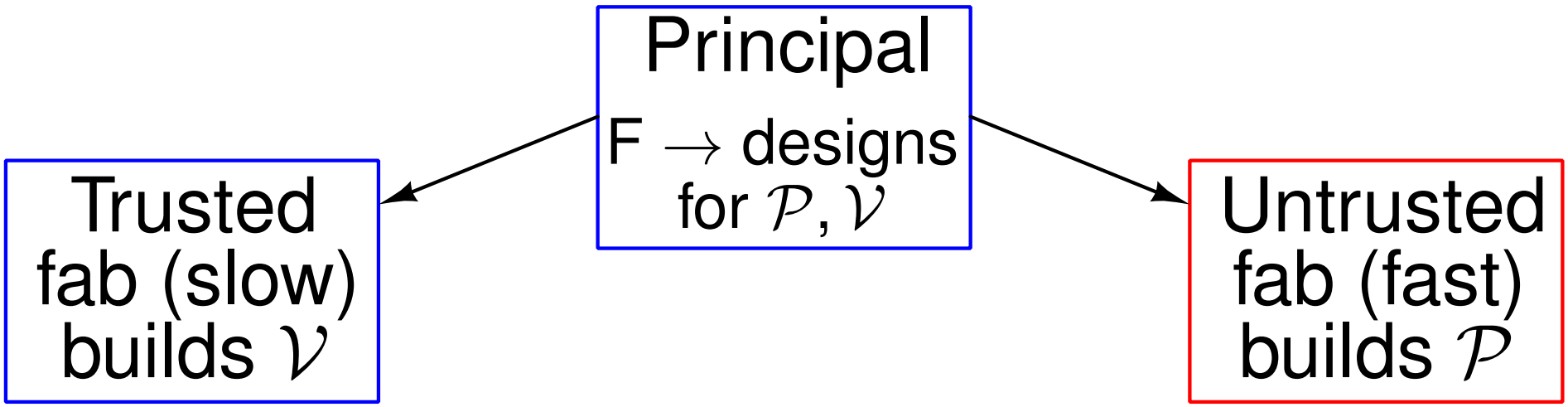
Can we get trust more cheaply?

Verifiable ASICs

Principal

F $\rightarrow$ designs for $\mathcal{P}, \mathcal{V}$

Verifiable ASICs



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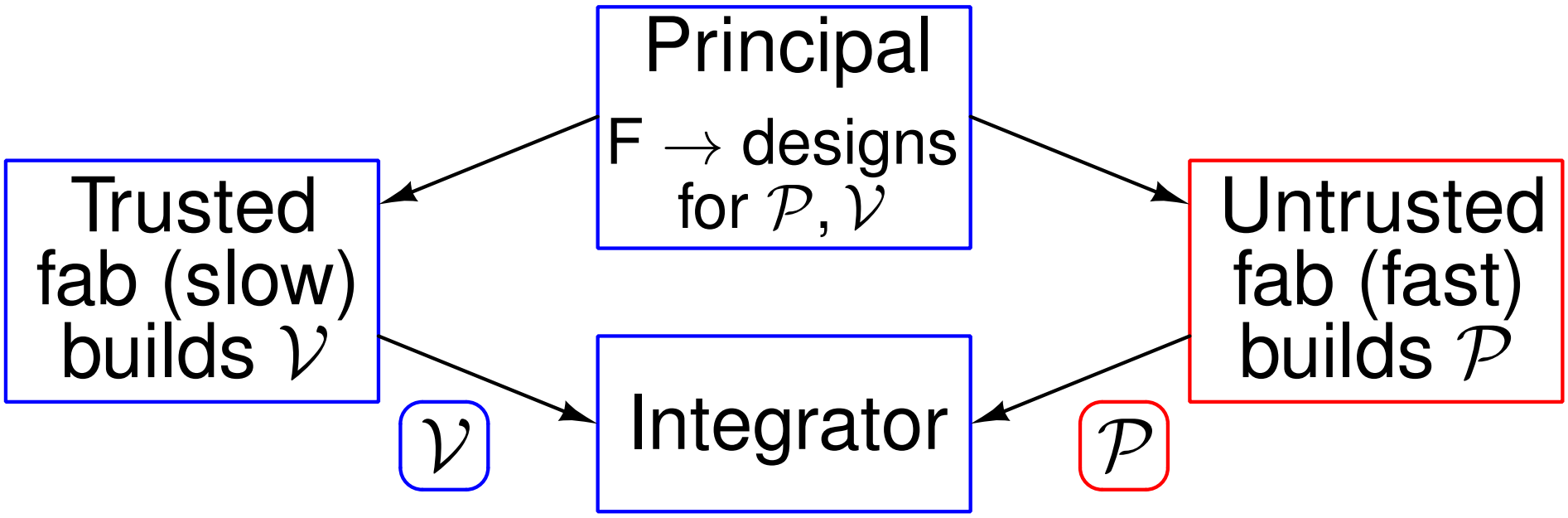

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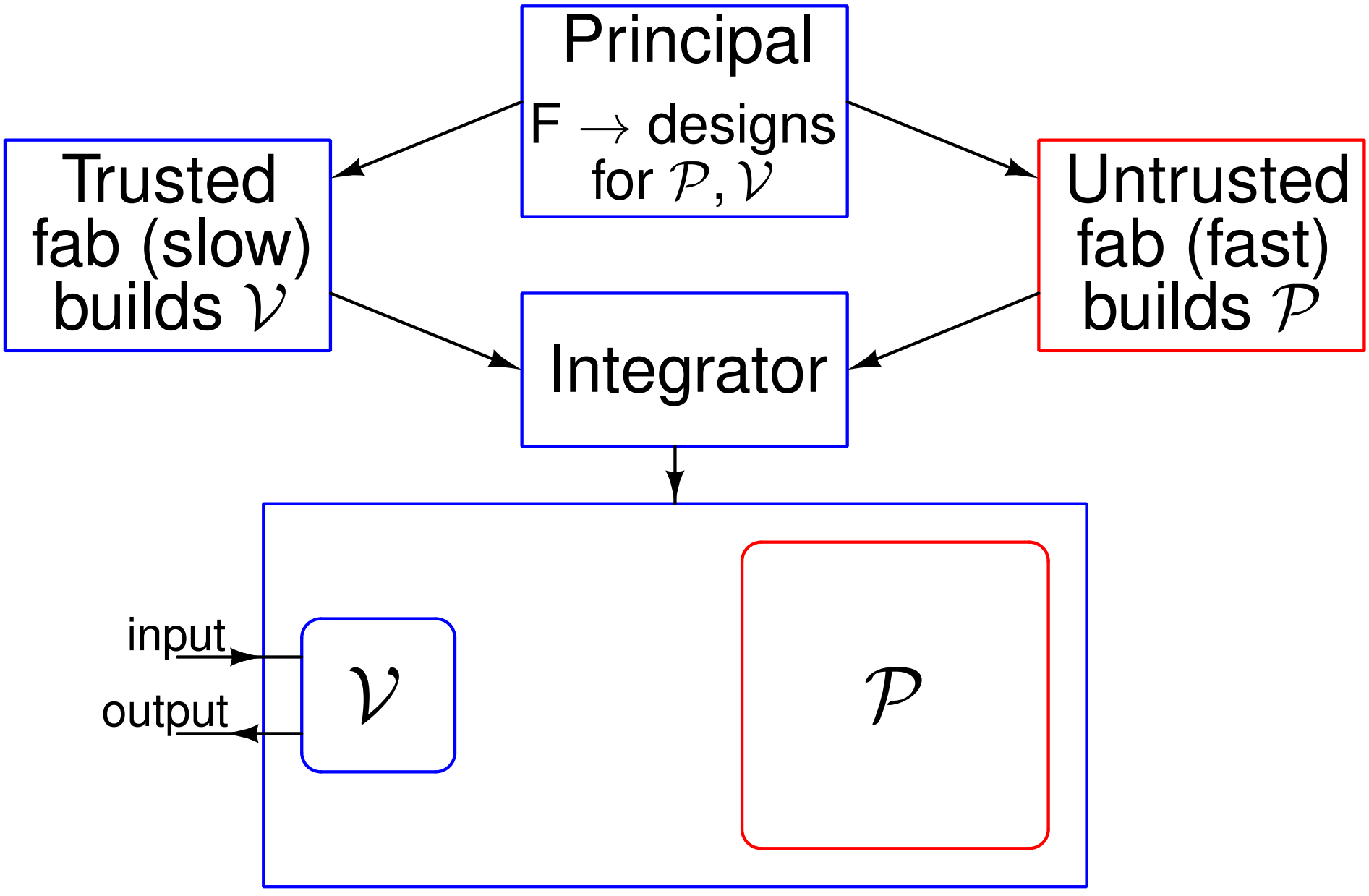

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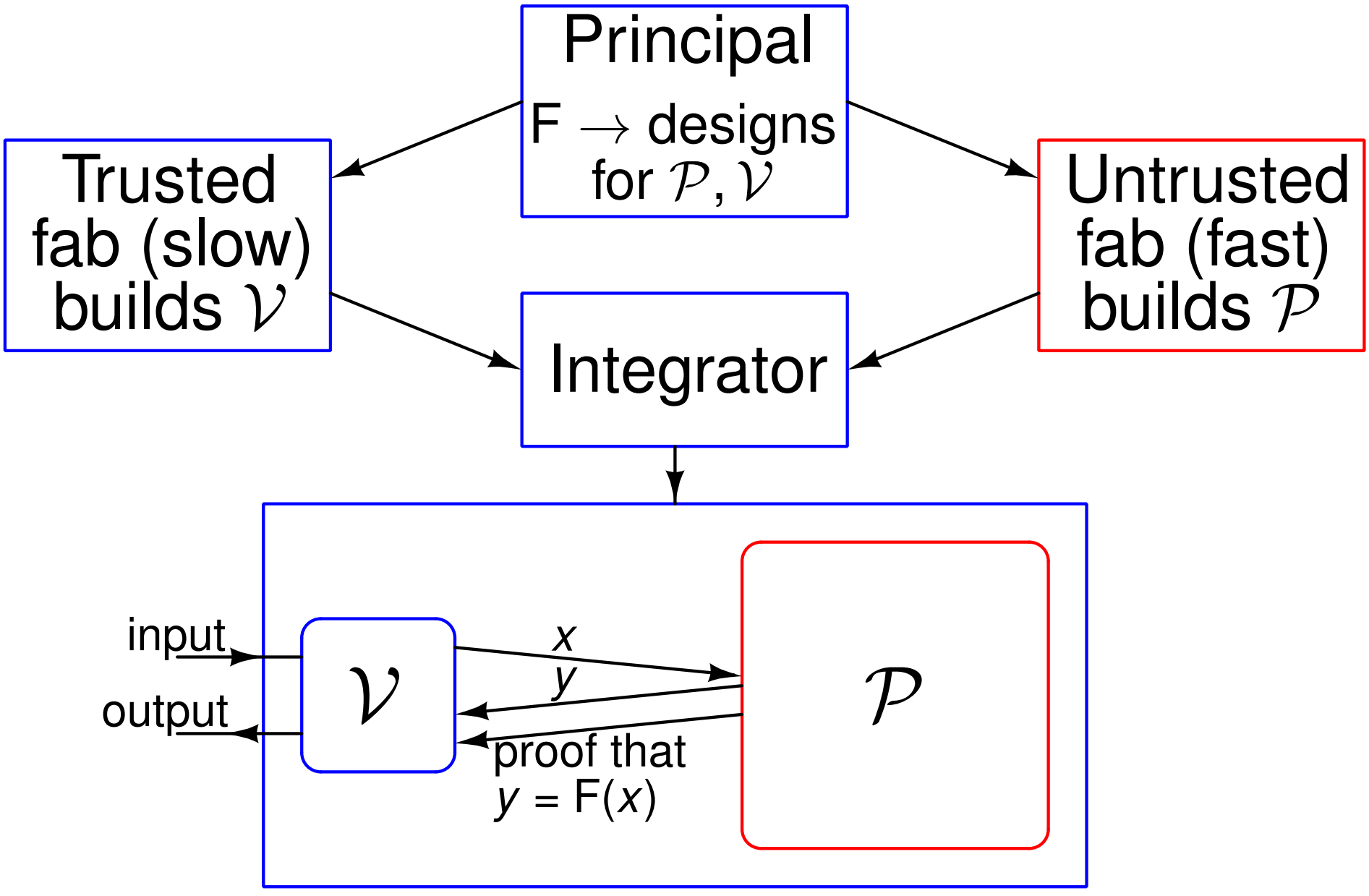
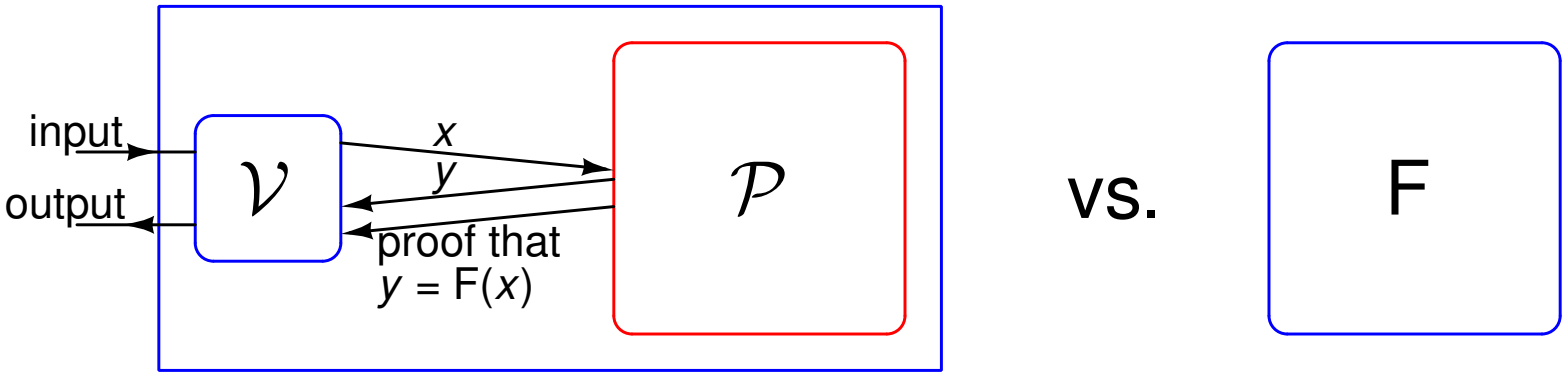


Can we build Verifiable ASICs?



Makes sense if $\mathcal{V} + \mathcal{P}$ are cheaper than trusted F

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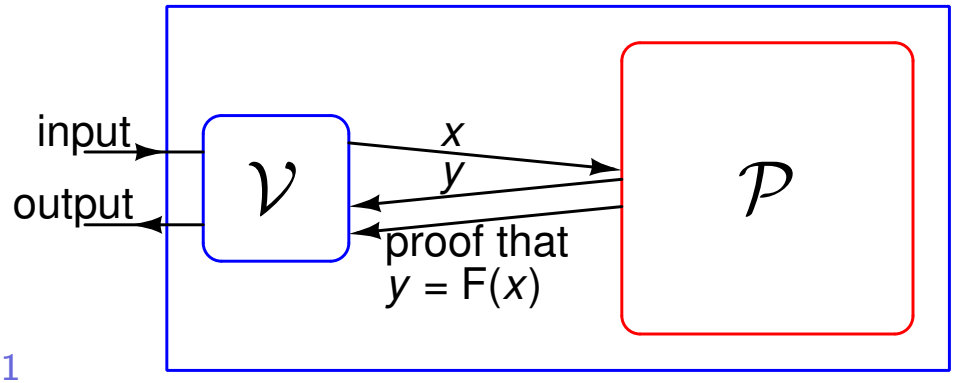

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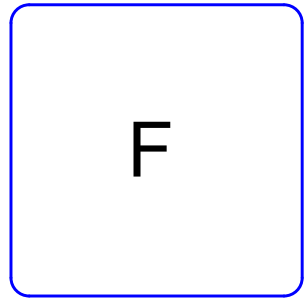

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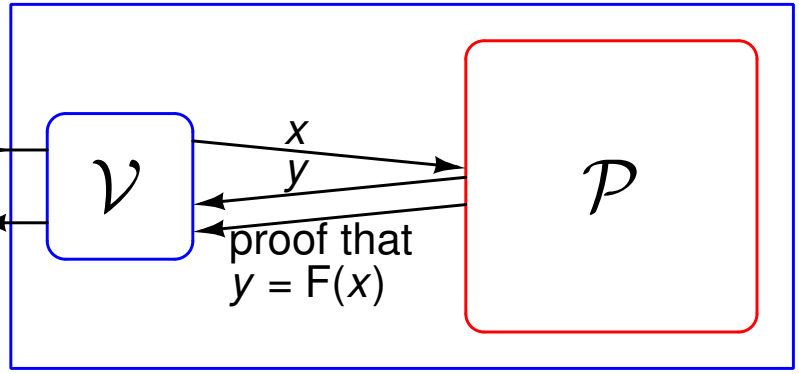

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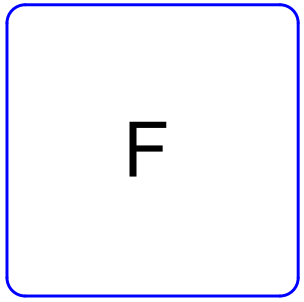

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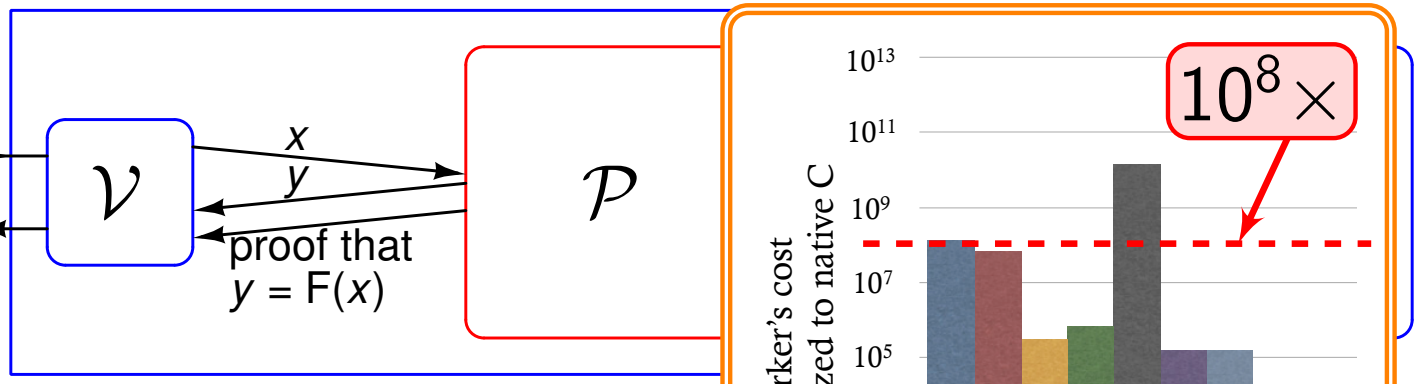

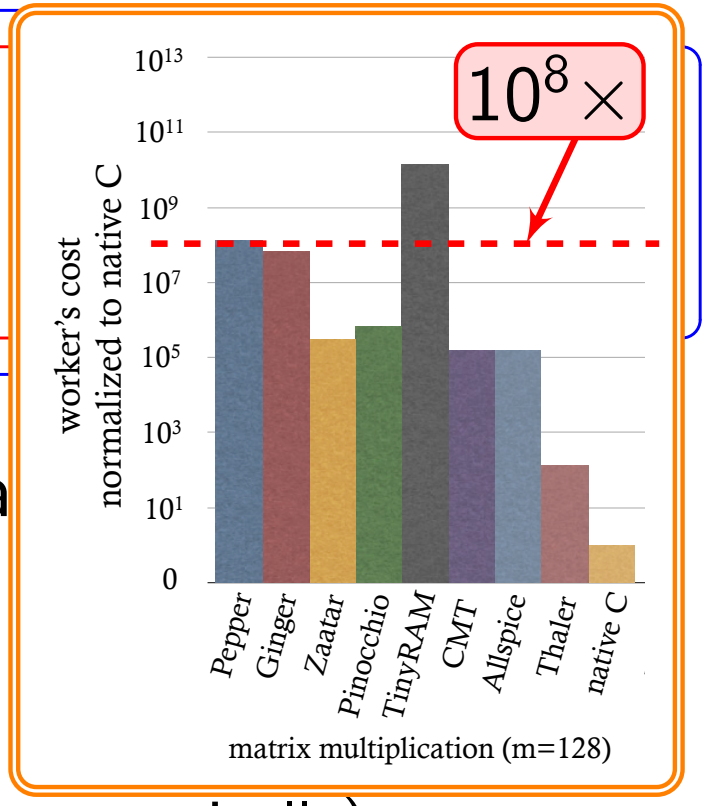

Makes sense if $\mathcal{V} + \mathcal{P}$ a
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- running time of $\mathcal{V} <$ F (ymptotically)
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- $\mathcal{P}$ overheads are massive, but using an advanced fab might offset these costs

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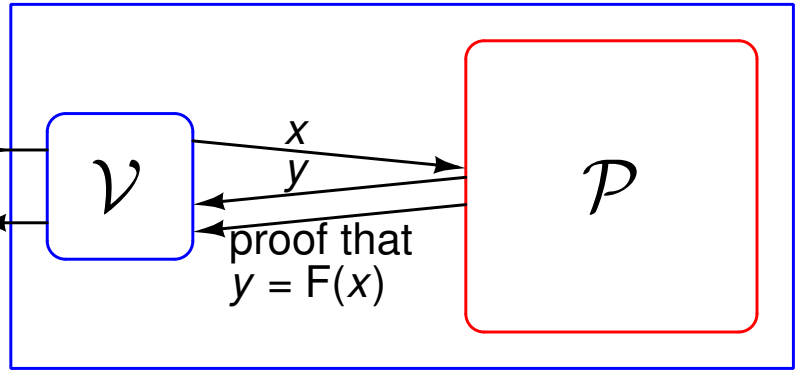

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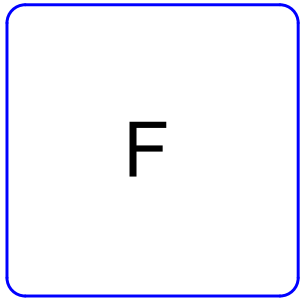

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Reasons for ~~hope~~ caution:

- Theory is silent about feasibility
- Onus is heavier than in prior work
- Hardware issues: energy, chip area
- Need physically realizable circuit design
- Need $\mathcal{V}$ to save for plausible computation sizes

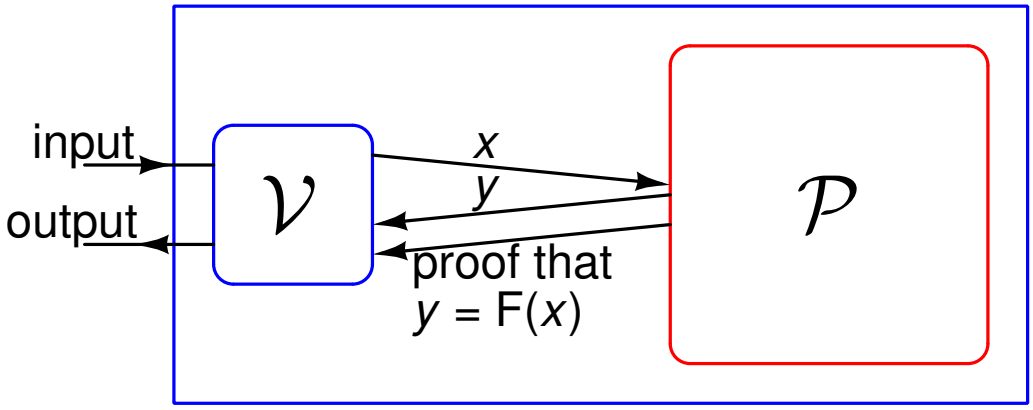
Zebra: a hardware design that saves costs

A **qualified** success

Zebra: a hardware design that saves costs...

...sometimes.

Probabilistic proof protocols, briefly

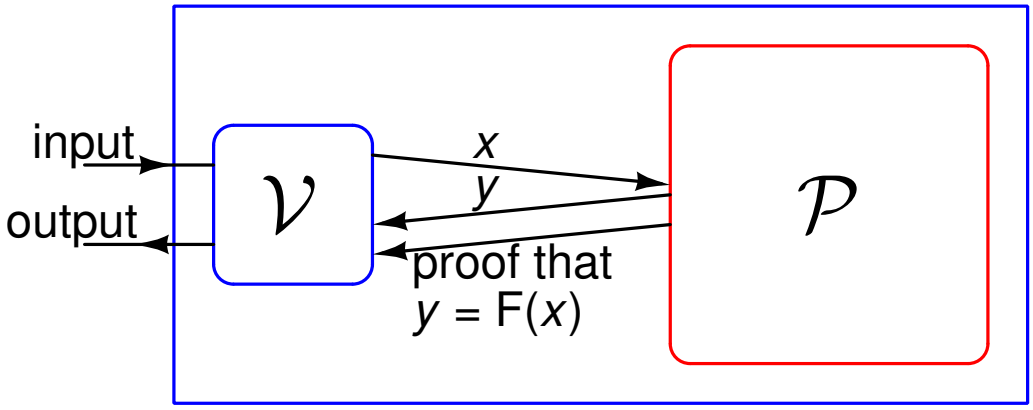


F must be expressed as an arithmetic circuit (AC)

AC satisfiable $\iff$ F was executed correctly

$\mathcal{P}$ convinces $\mathcal{V}$ that the AC is satisfiable

Probabilistic proof protocols, briefly



Arguments [GGPR13, SBVBPW13, PGHR13, BCTV14]

e.g., Zaatar, Pinocchio, libsnark

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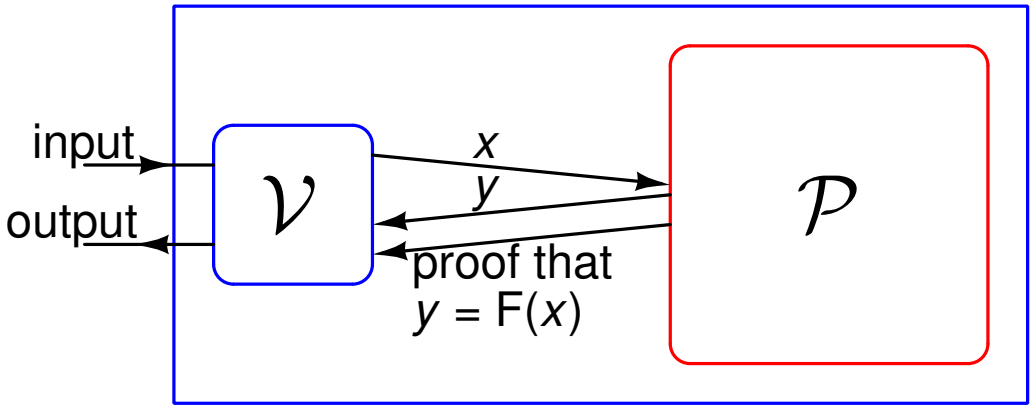

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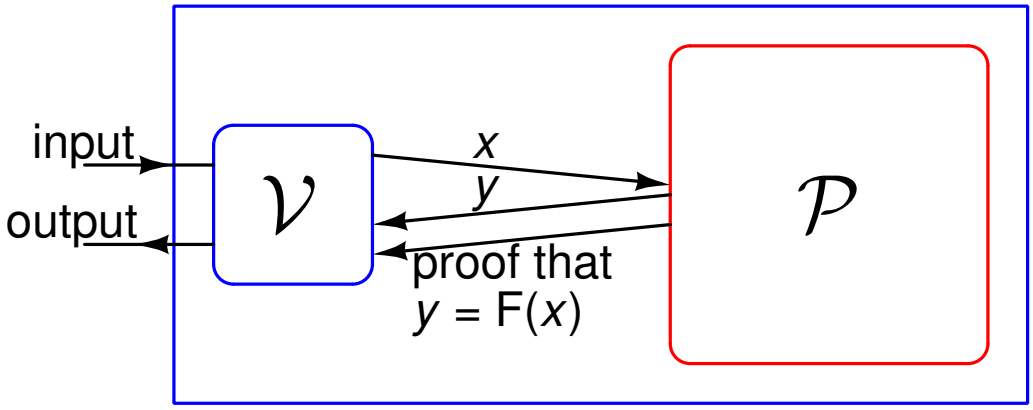

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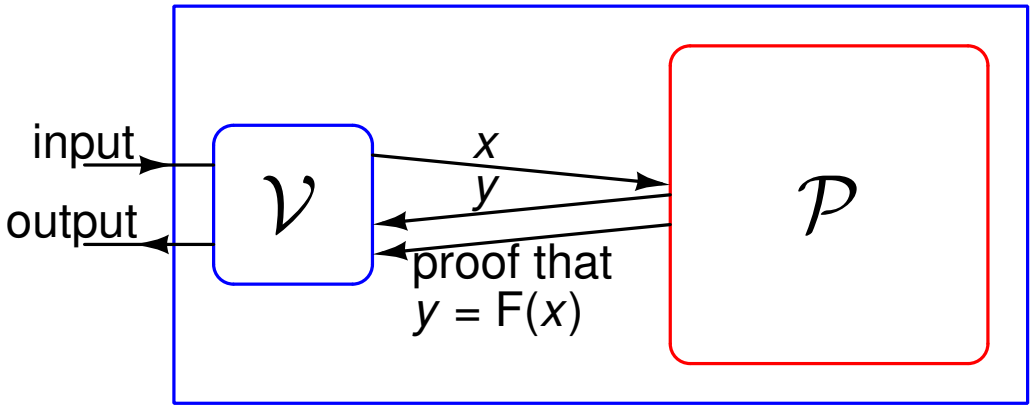
These all seem a bit further from practicality.

Probabilistic proof protocols, briefly



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\+ nondeterministic ACs, arbitrary connectivity

\+ Few rounds (≤ 3)

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– deterministic ACs; layered, low depth

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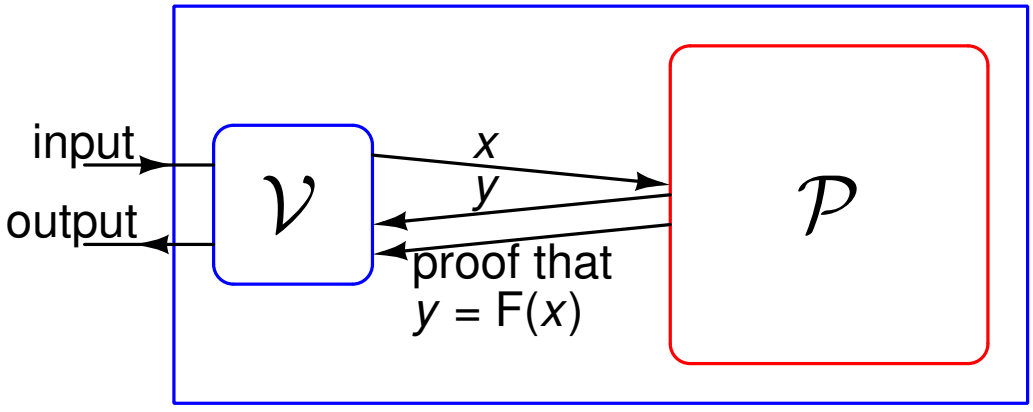

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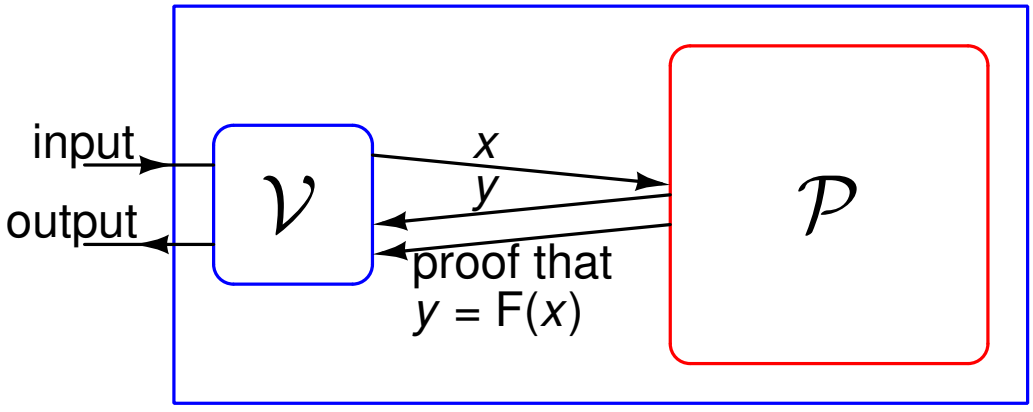

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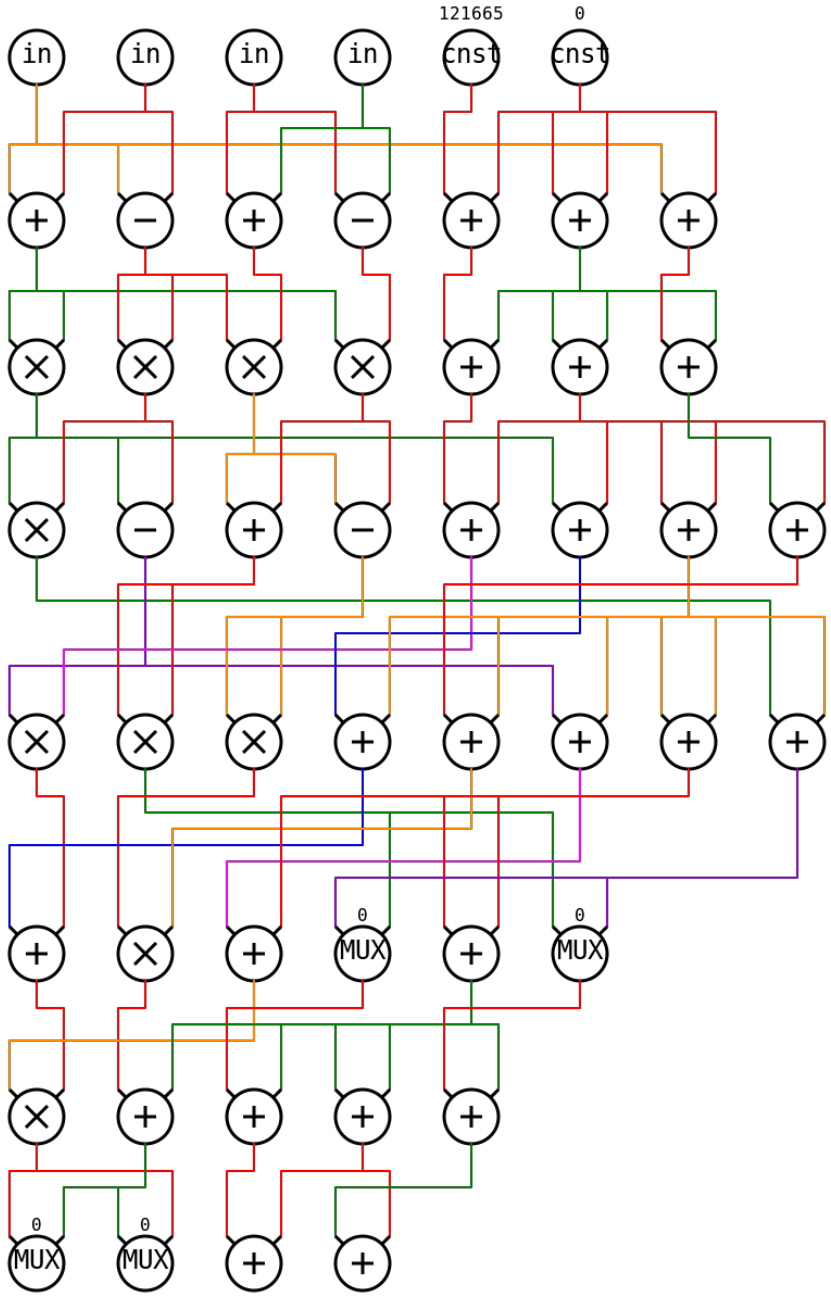
Suited to hardware implementation ✓

Zebra builds on IPs of GKR [GKR08, CMT12, VSBW13]

F must be expressed as a *layered* arithmetic circuit.



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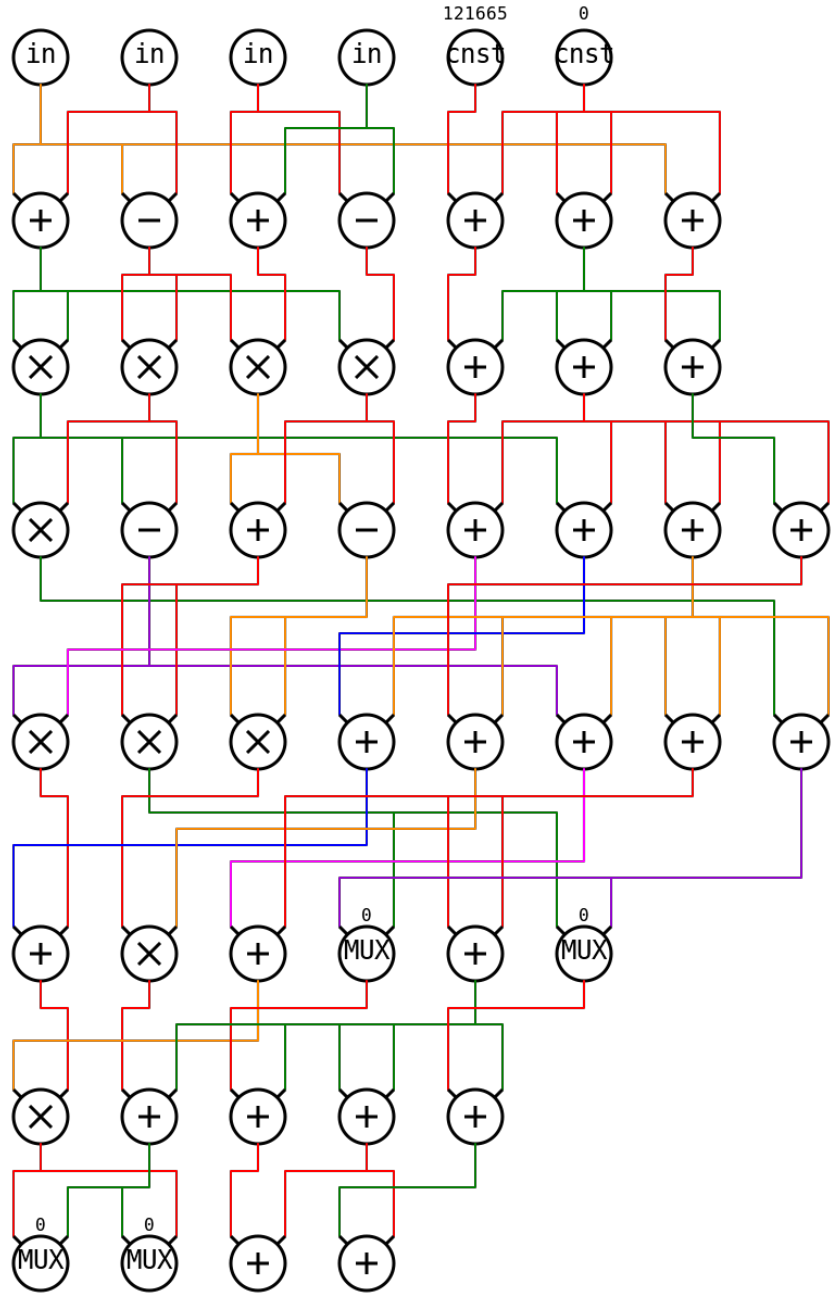

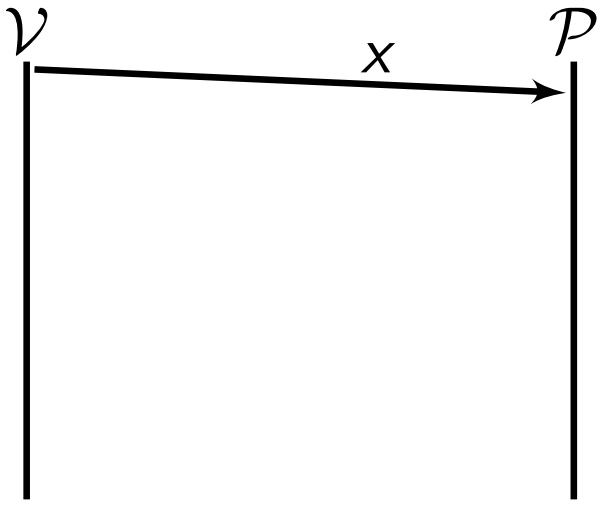

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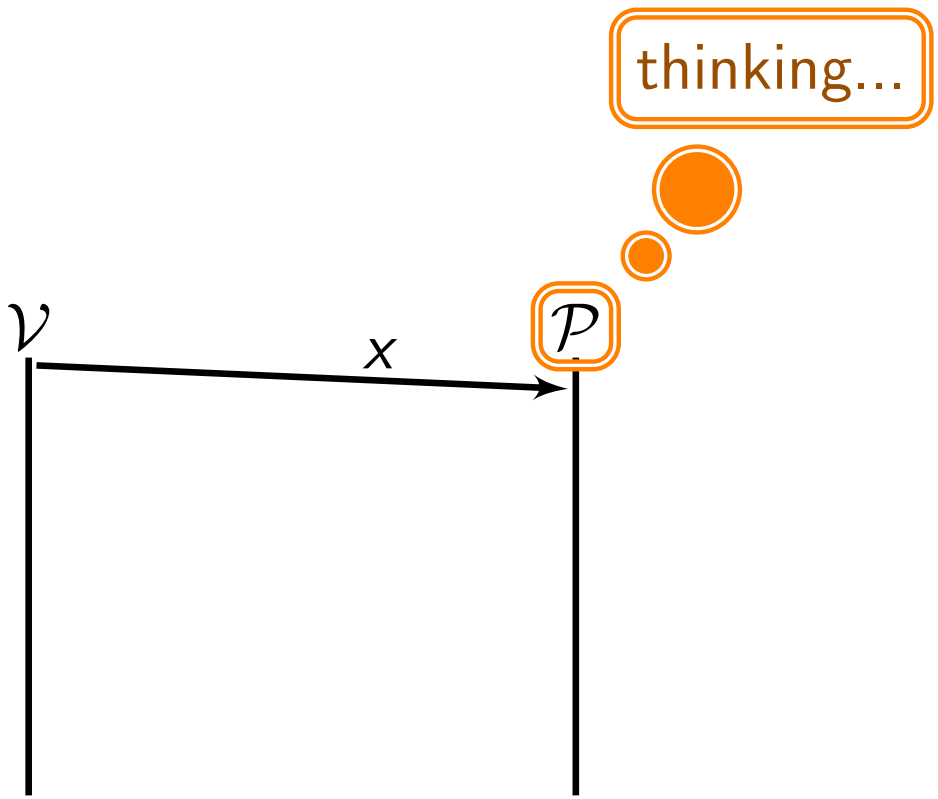

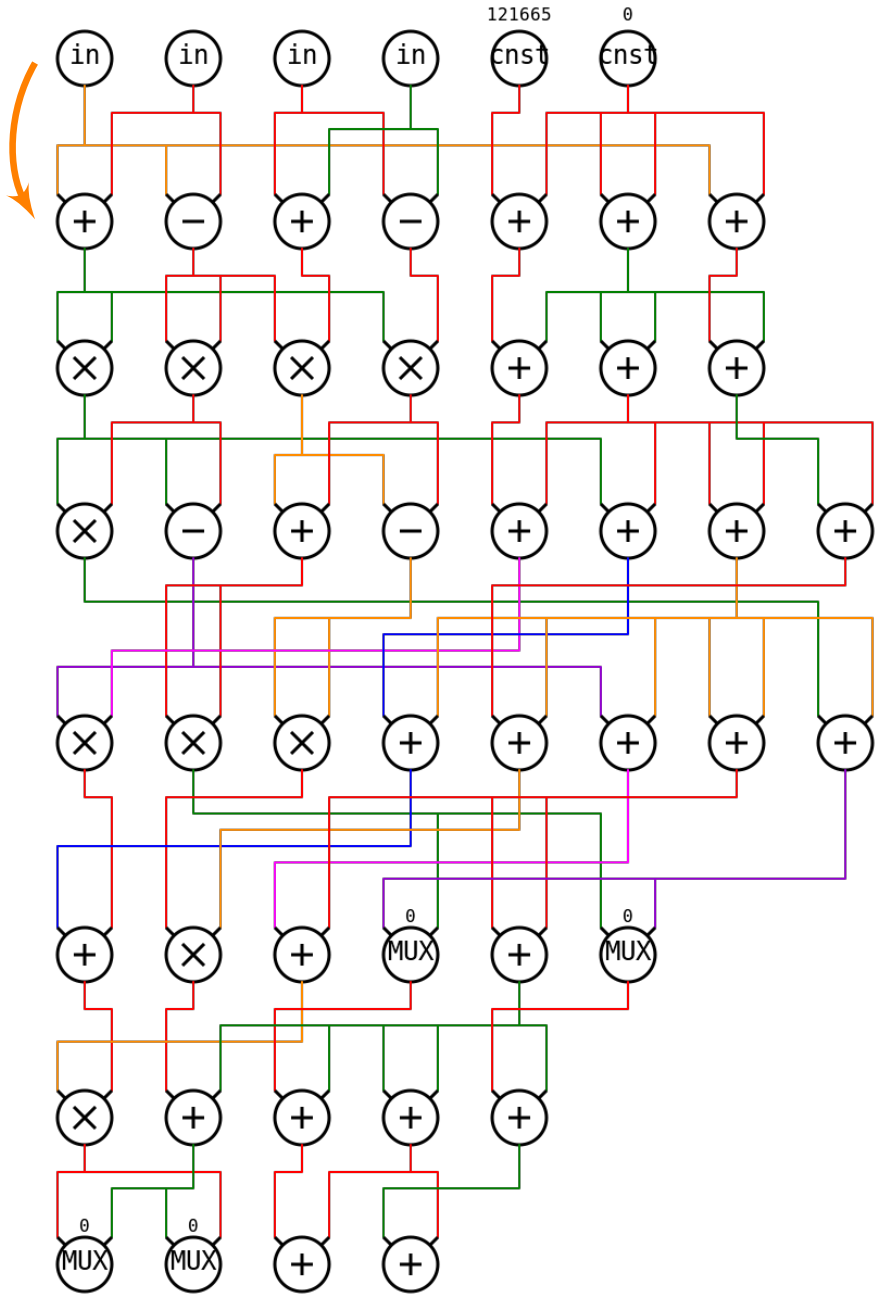

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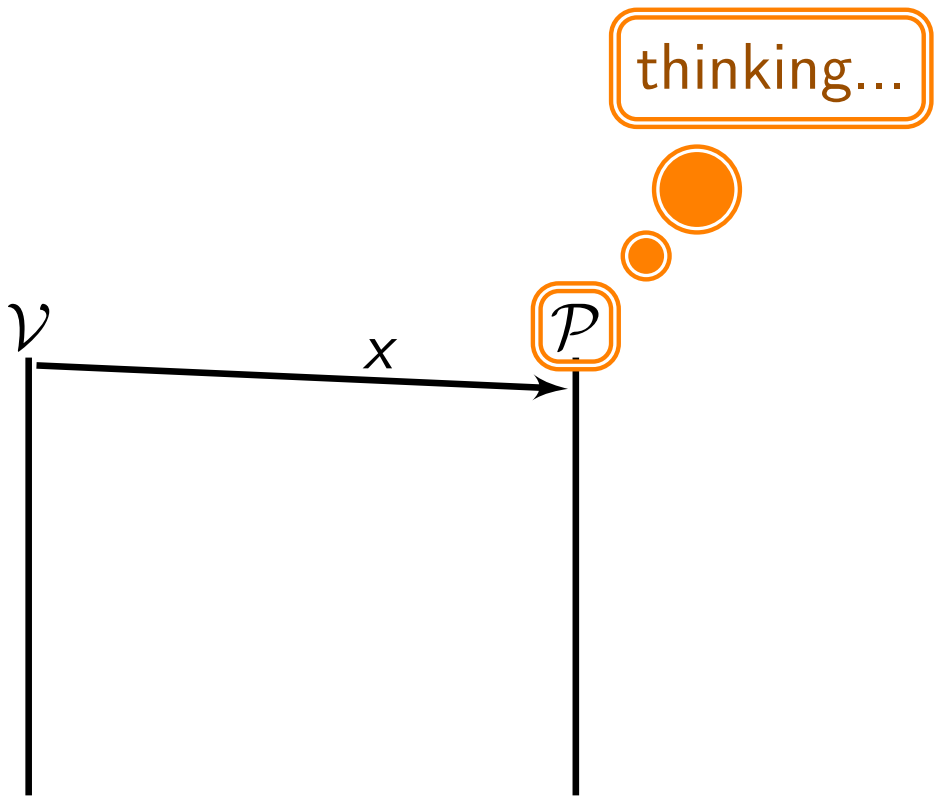

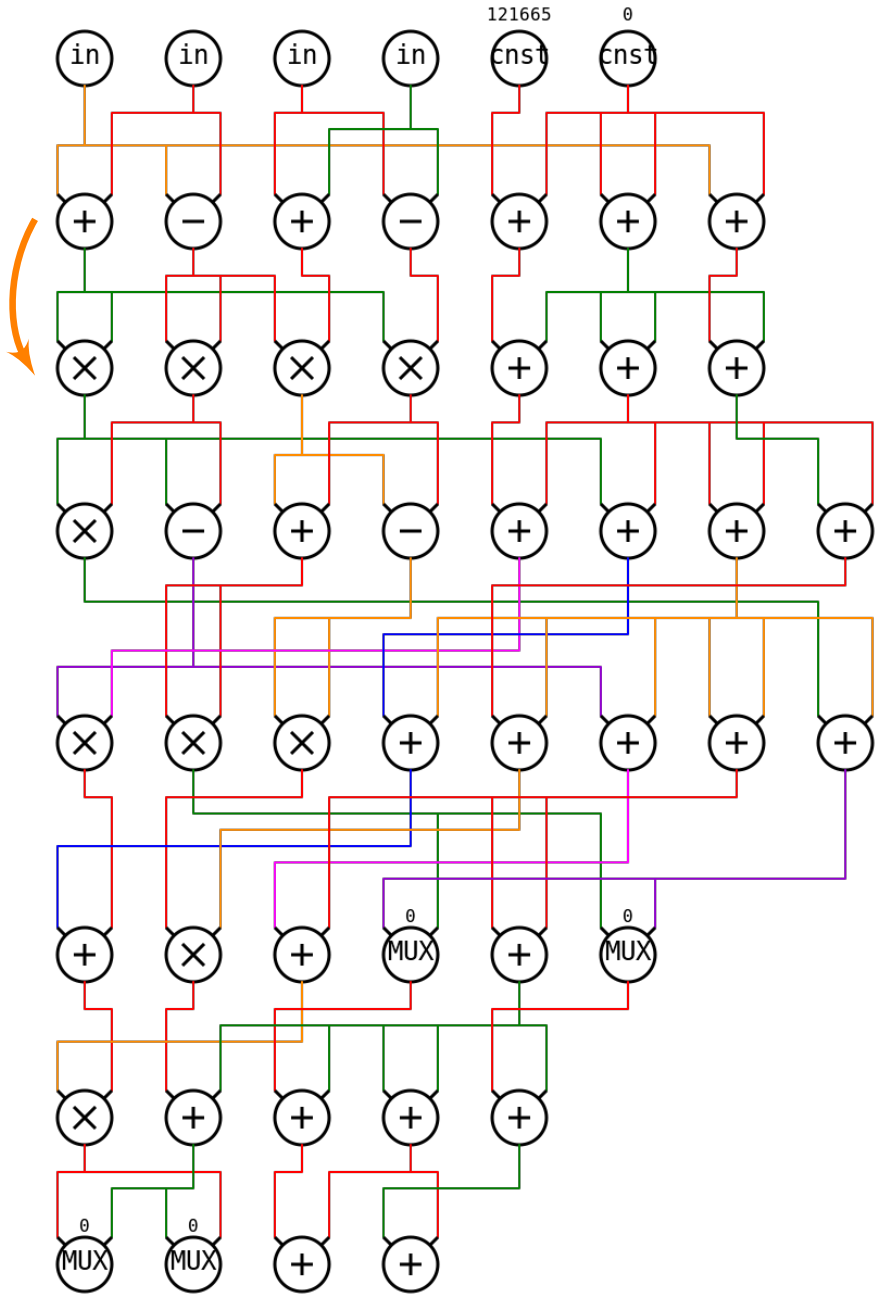

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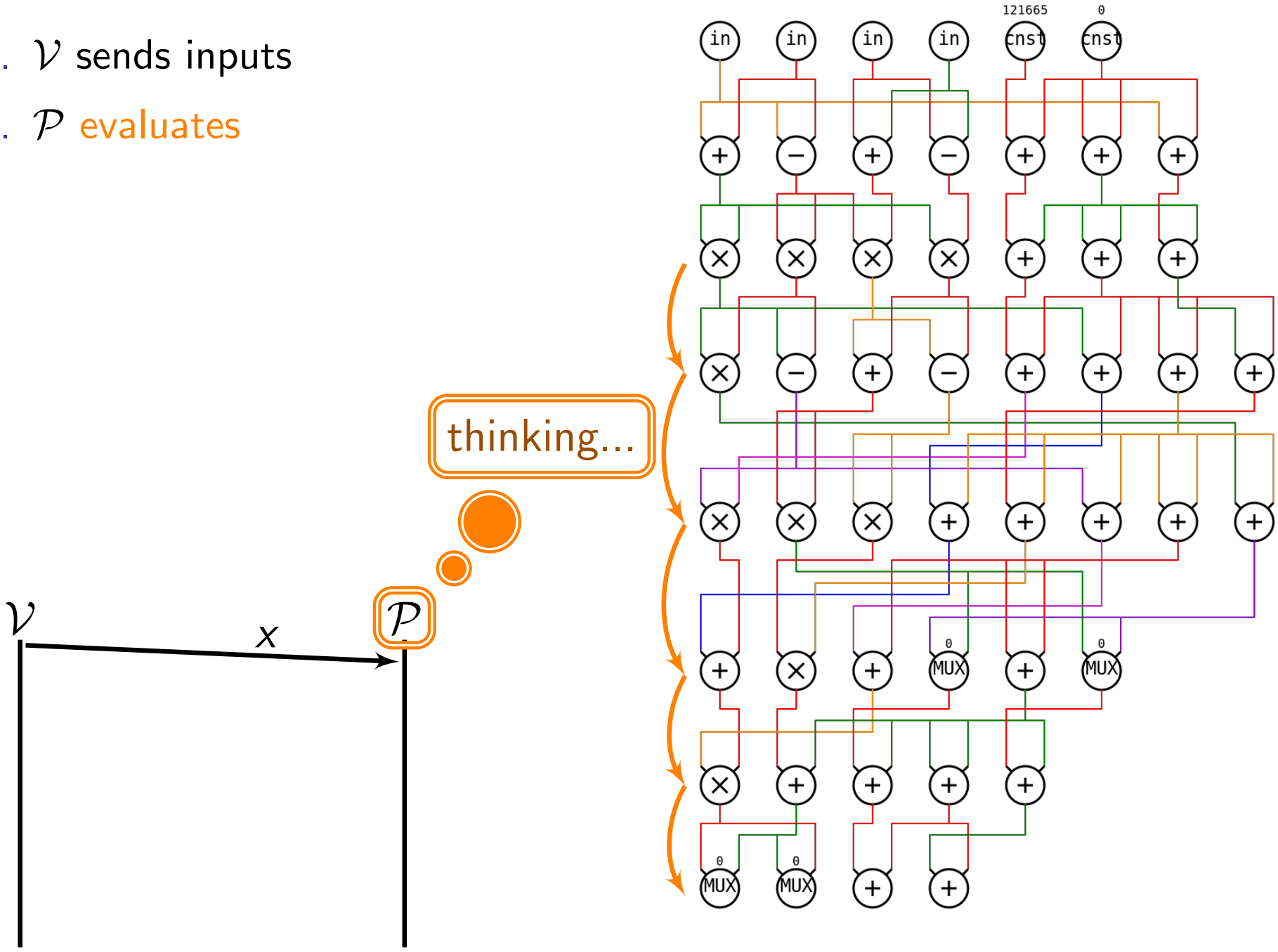
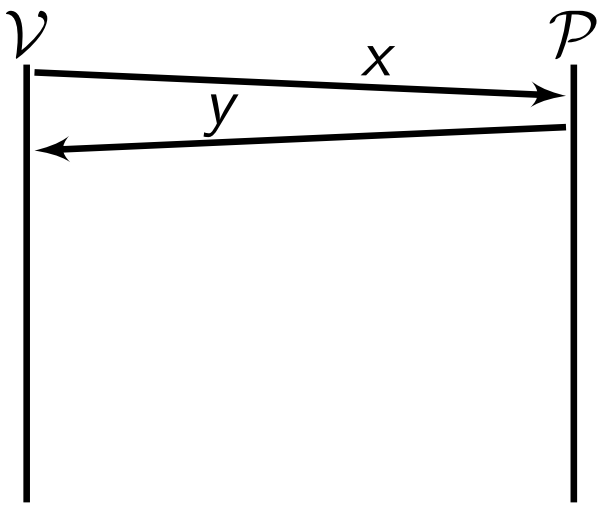
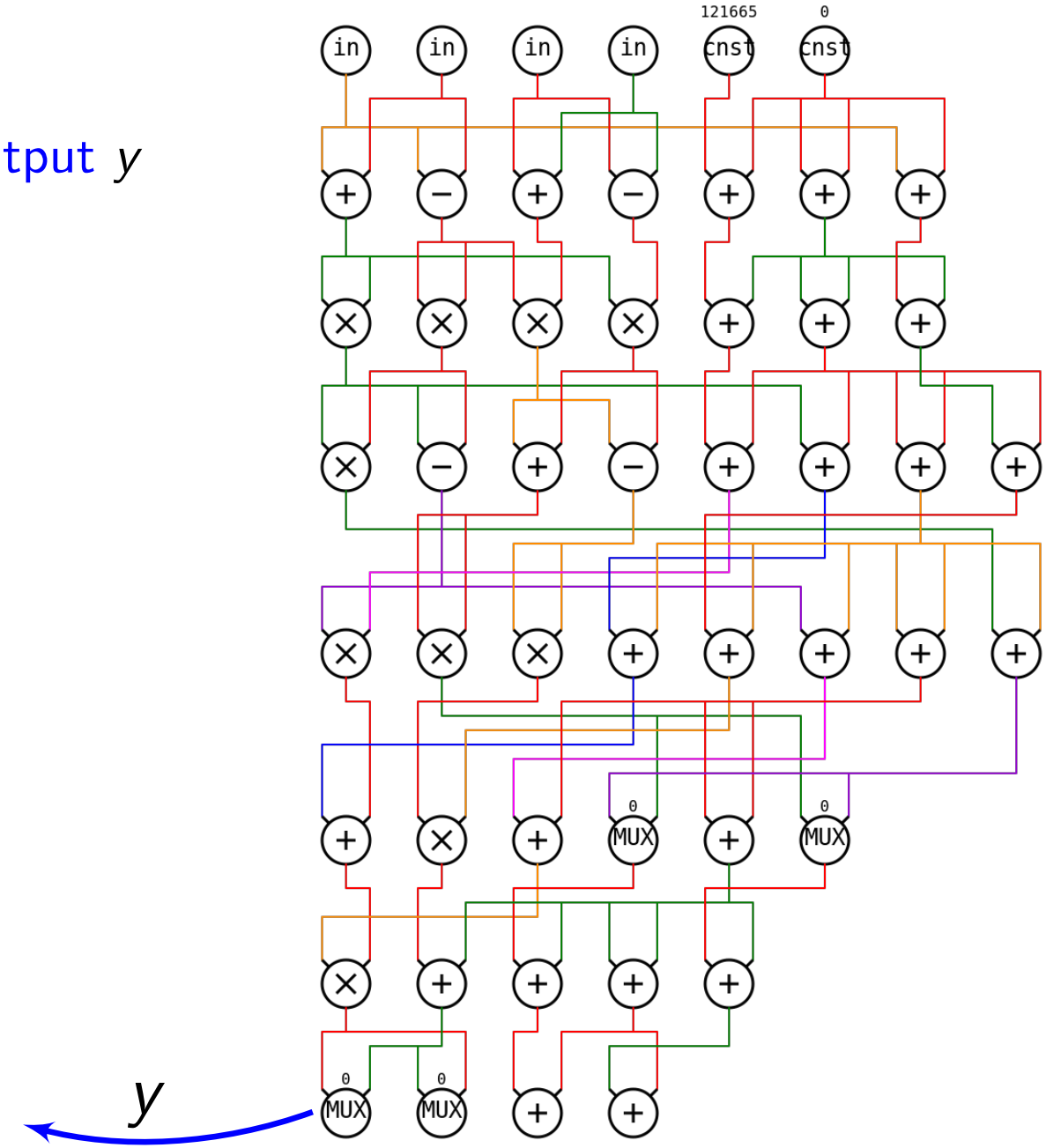


Zebra builds on IPs of GKR [GKR08, CMT12, VSBW13]

1. $\mathcal{V}$ sends inputs
2. $\mathcal{P}$ evaluates, returns output y





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1. $\mathcal{V}$ sends inputs
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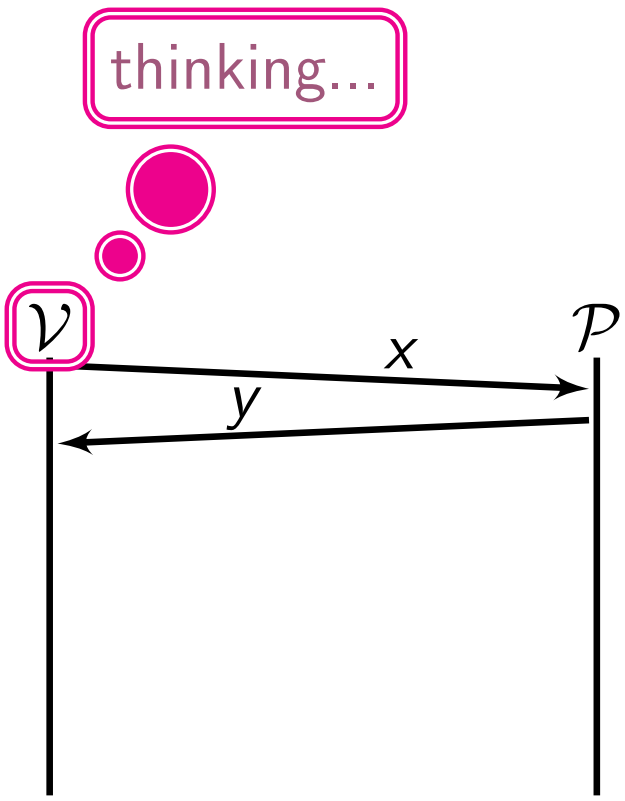
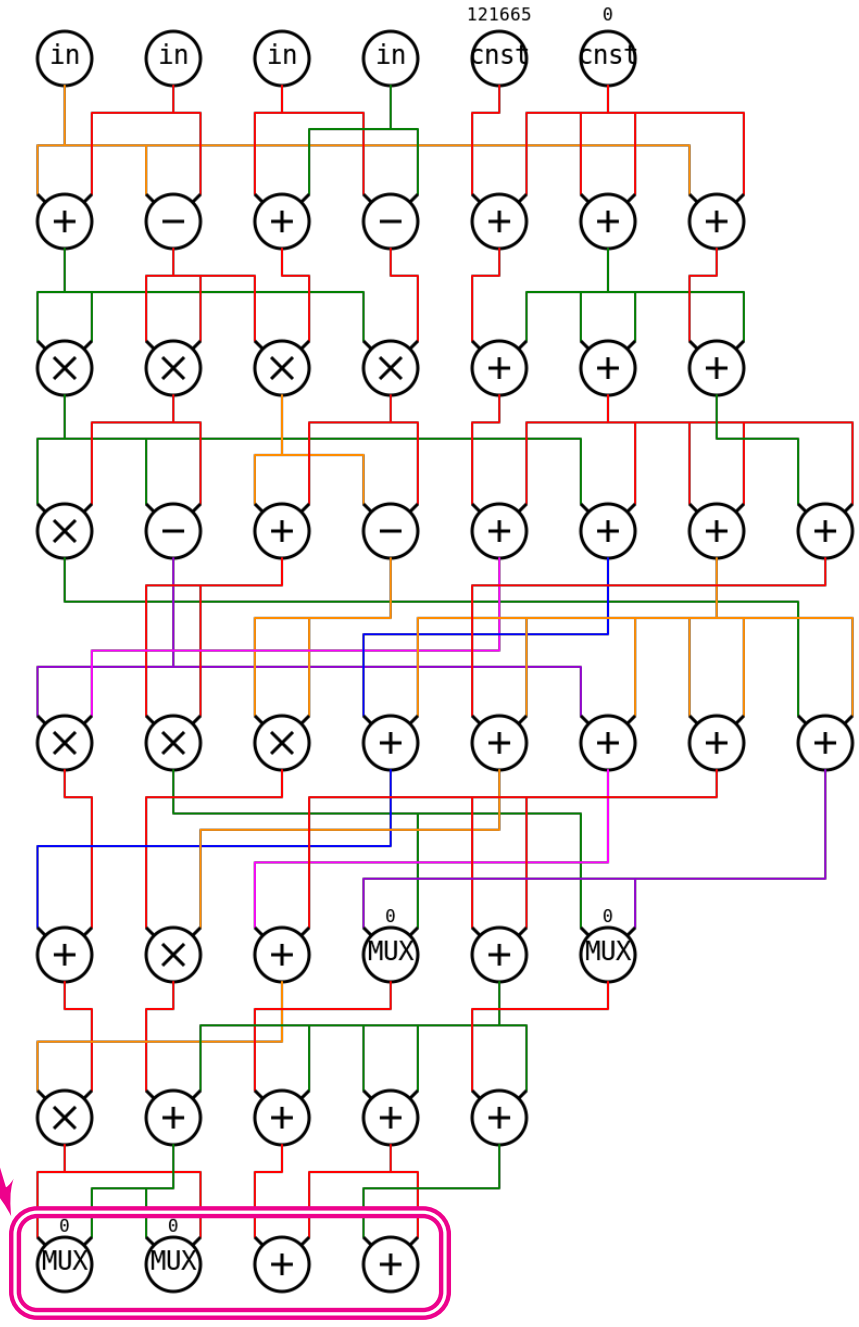
3. $\mathcal{V}$ constructs polynomial relating y to last layer's input wires





Zebra builds on IPs of GKR [GKR08, CMT12, VSBW13]

1. $\mathcal{V}$ sends inputs
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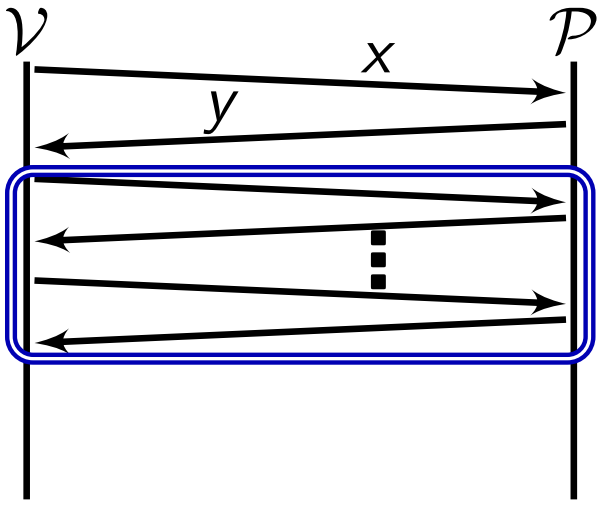
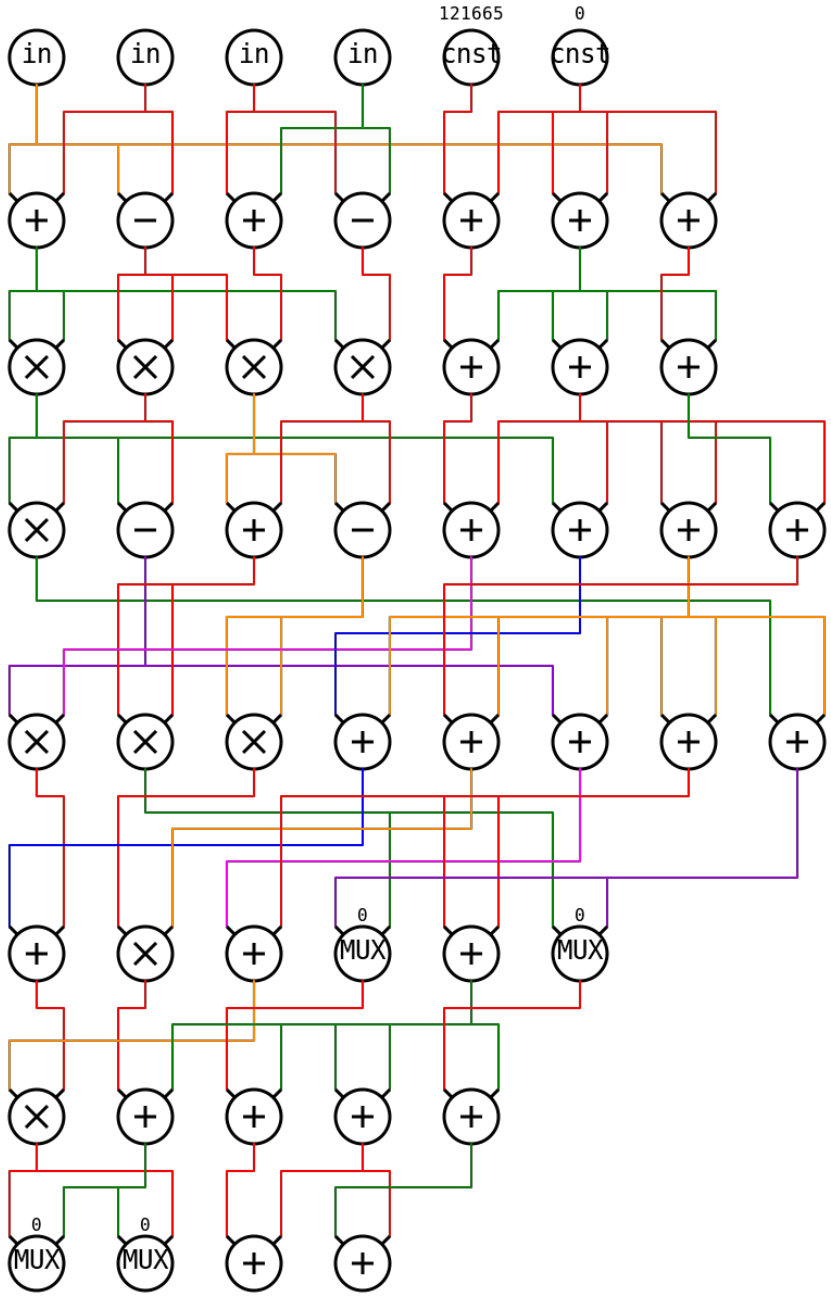
4. $\mathcal{V}$ engages $\mathcal{P}$ in a sum-check



sum-check [LFKN90]



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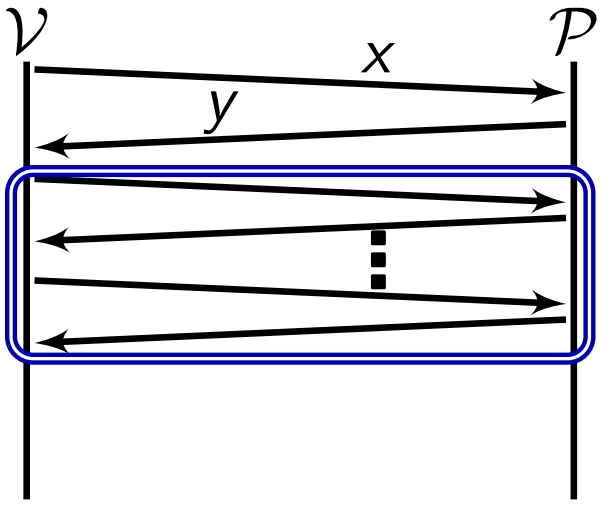

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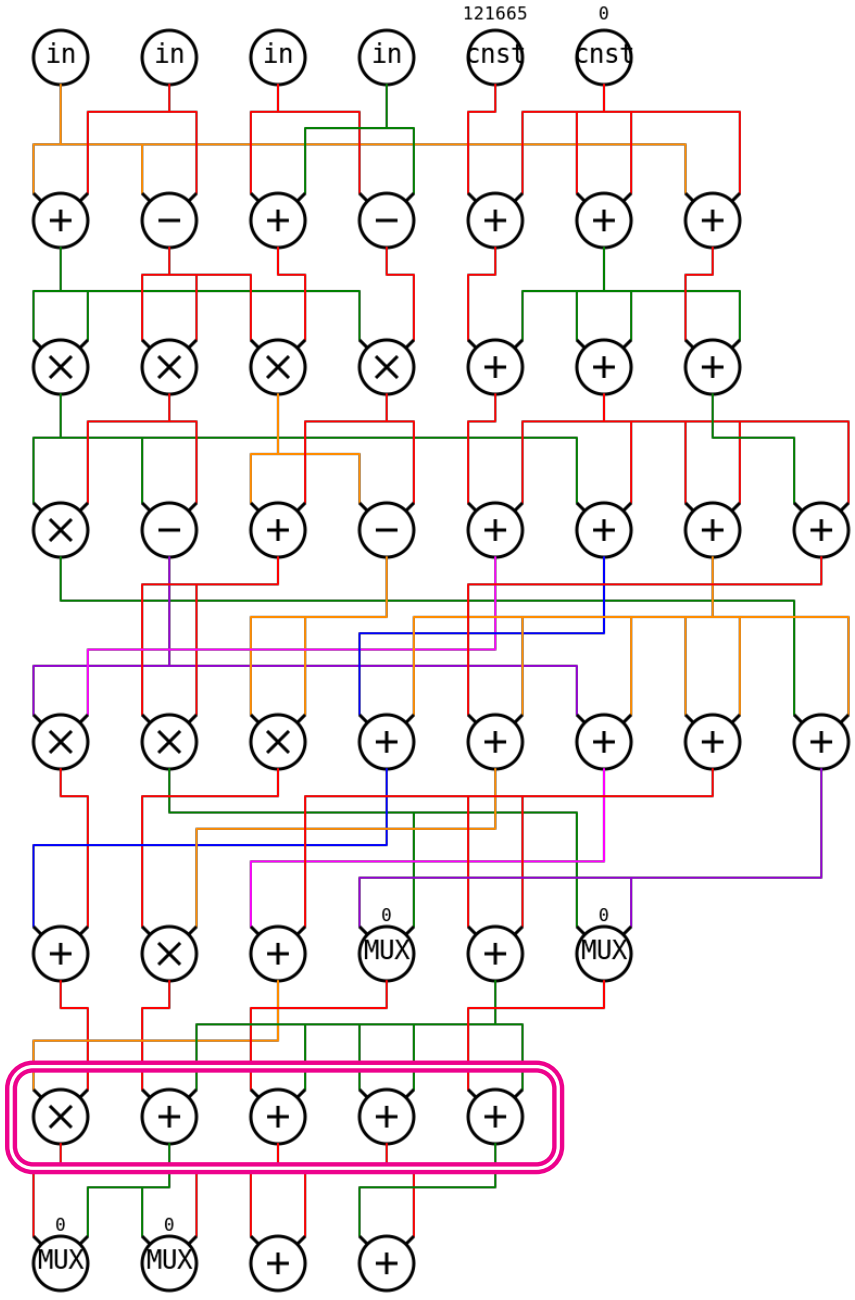

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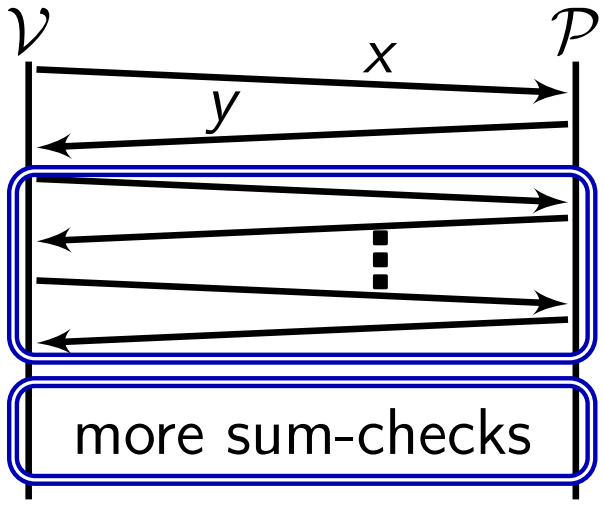

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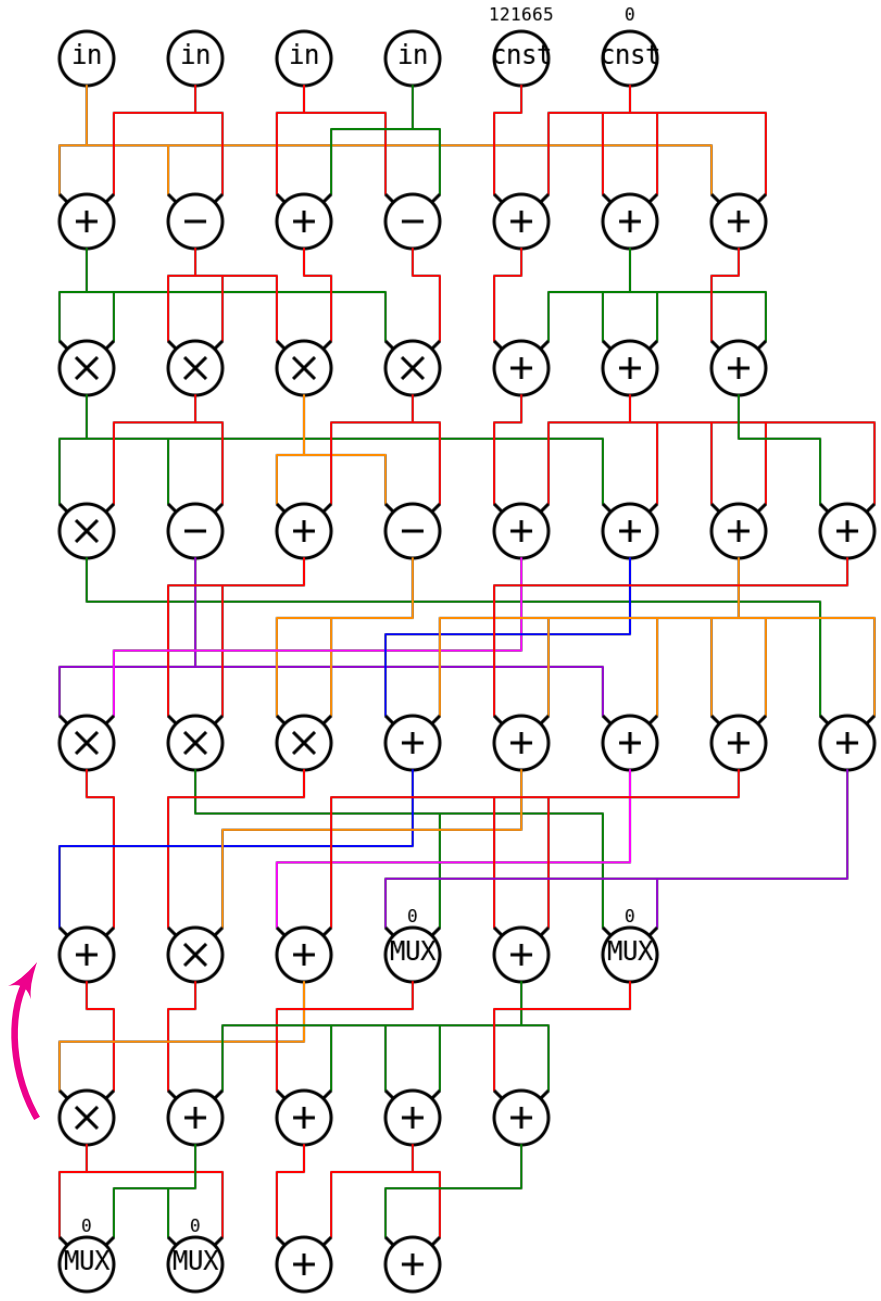

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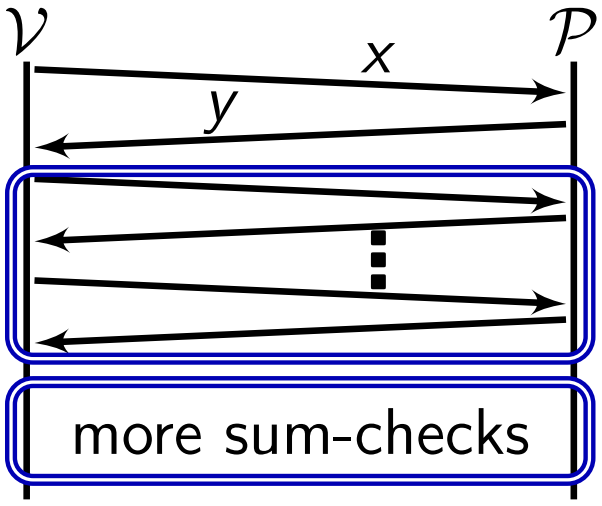

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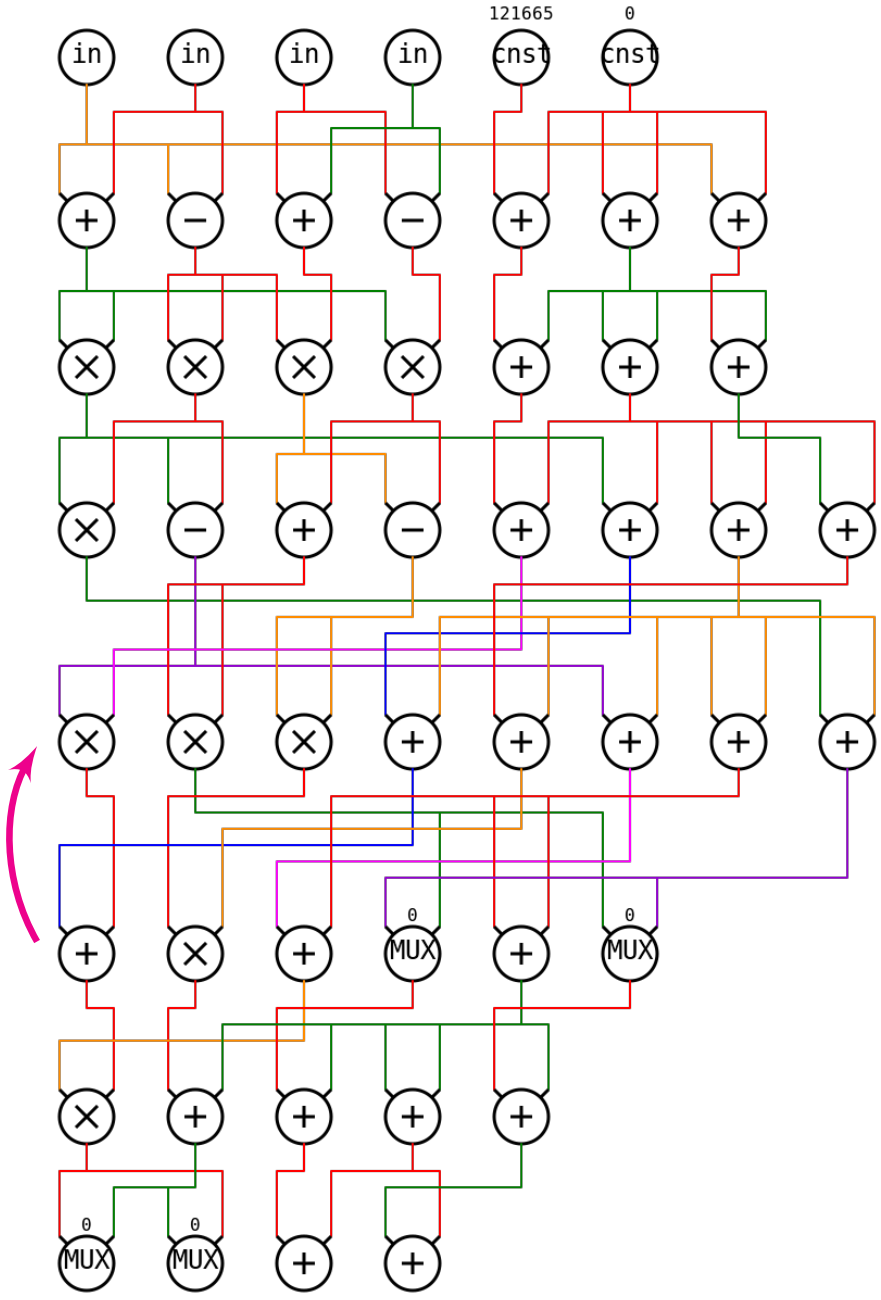

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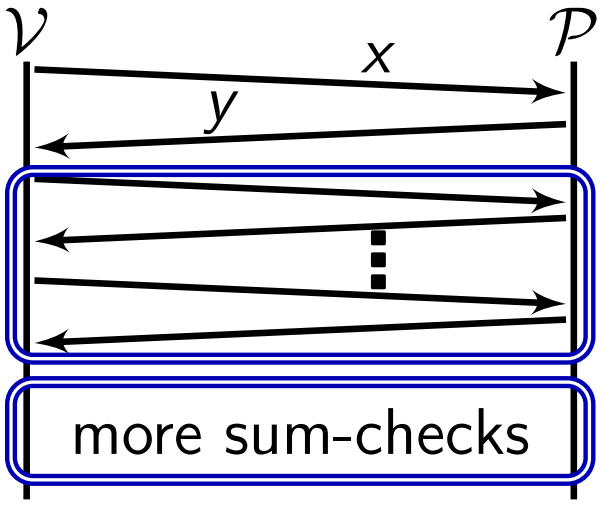

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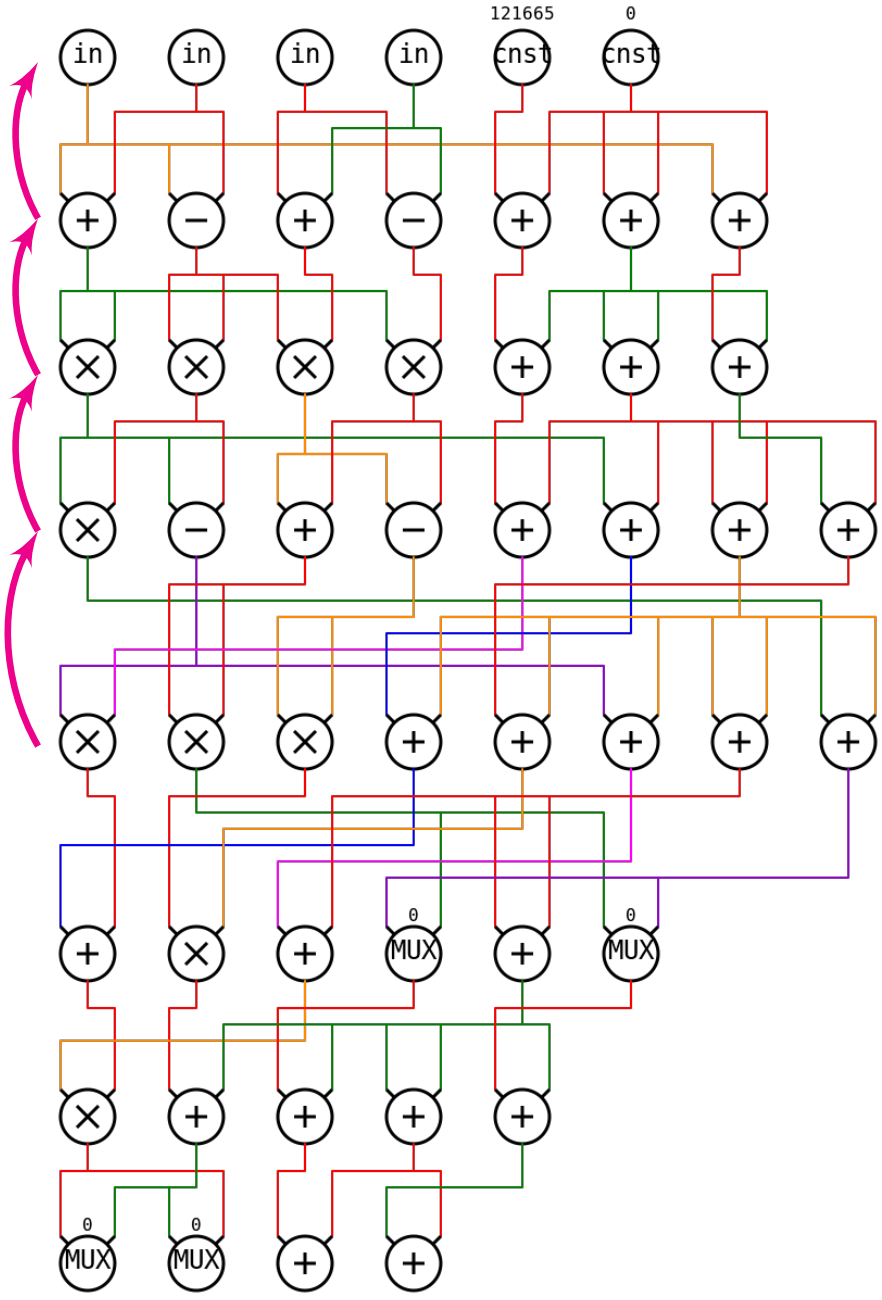

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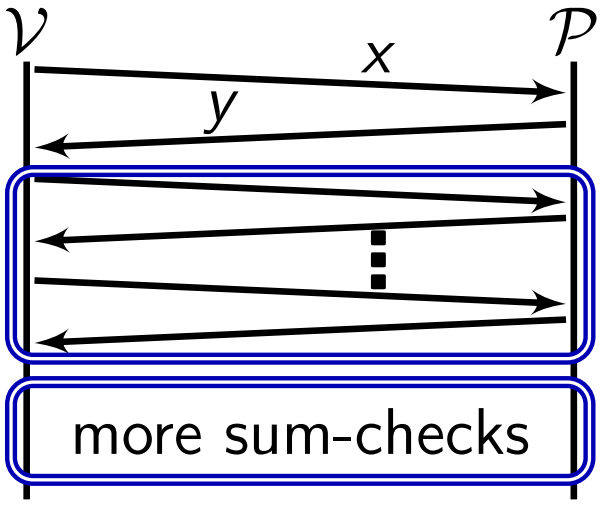
4. $\mathcal{V}$ engages $\mathcal{P}$ in a sum-check, gets claim about second-last layer
5. $\mathcal{V}$ iterates, gets claim about inputs, which it can check



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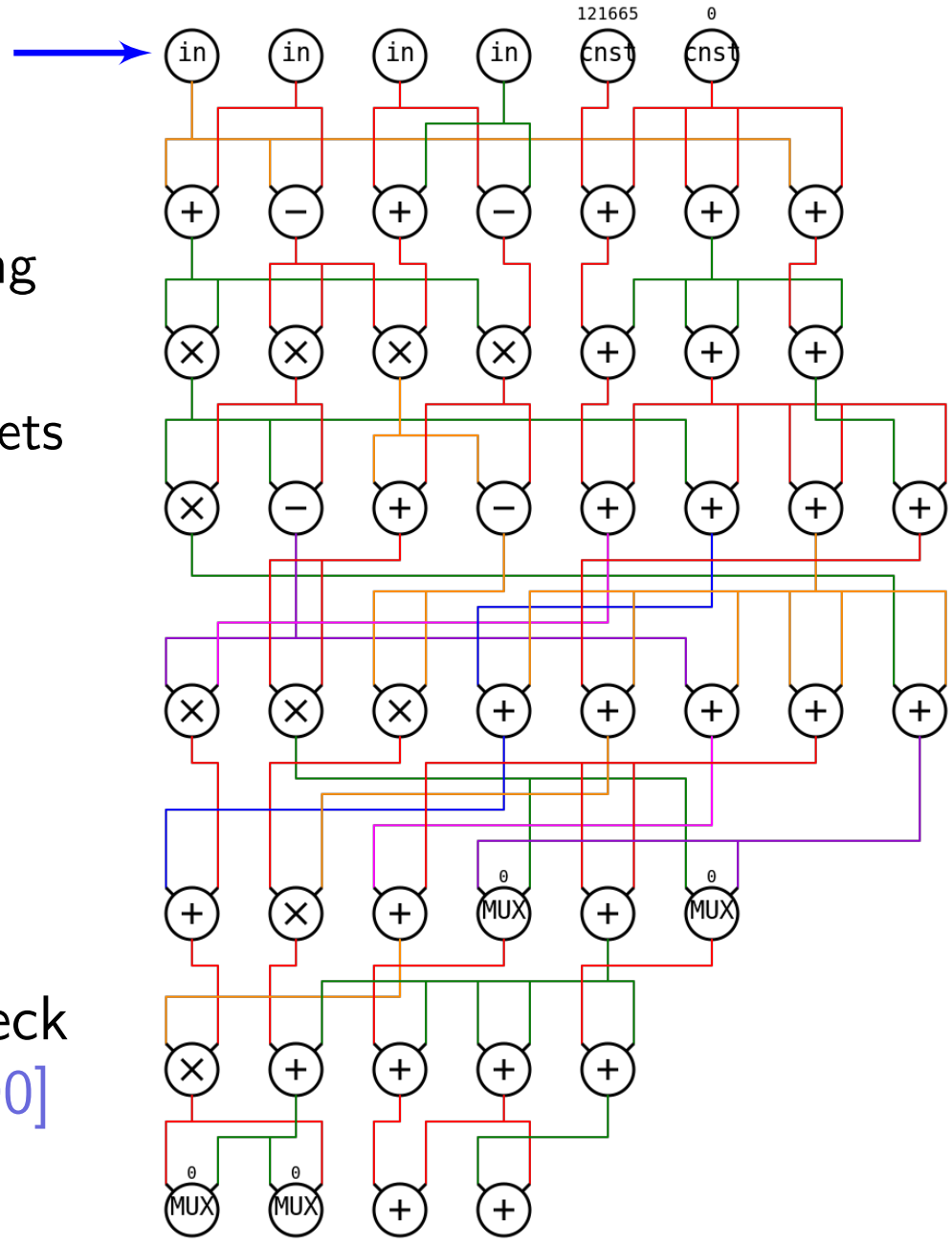
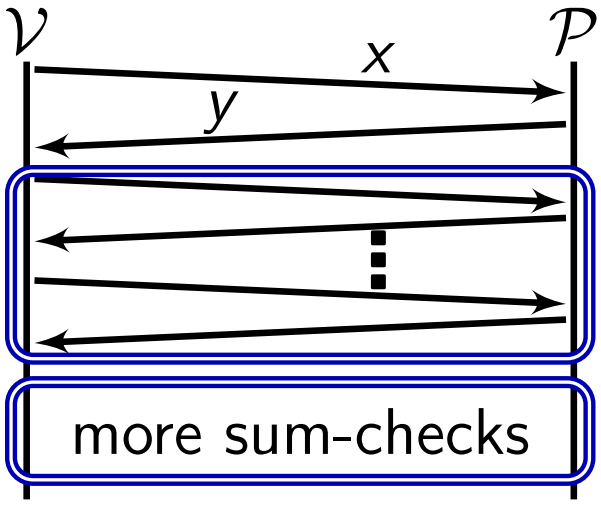


Zebra builds on IPs of GKR [GKR08, CMT12, VSBW13]

Soundness error $\propto p^{-1}$



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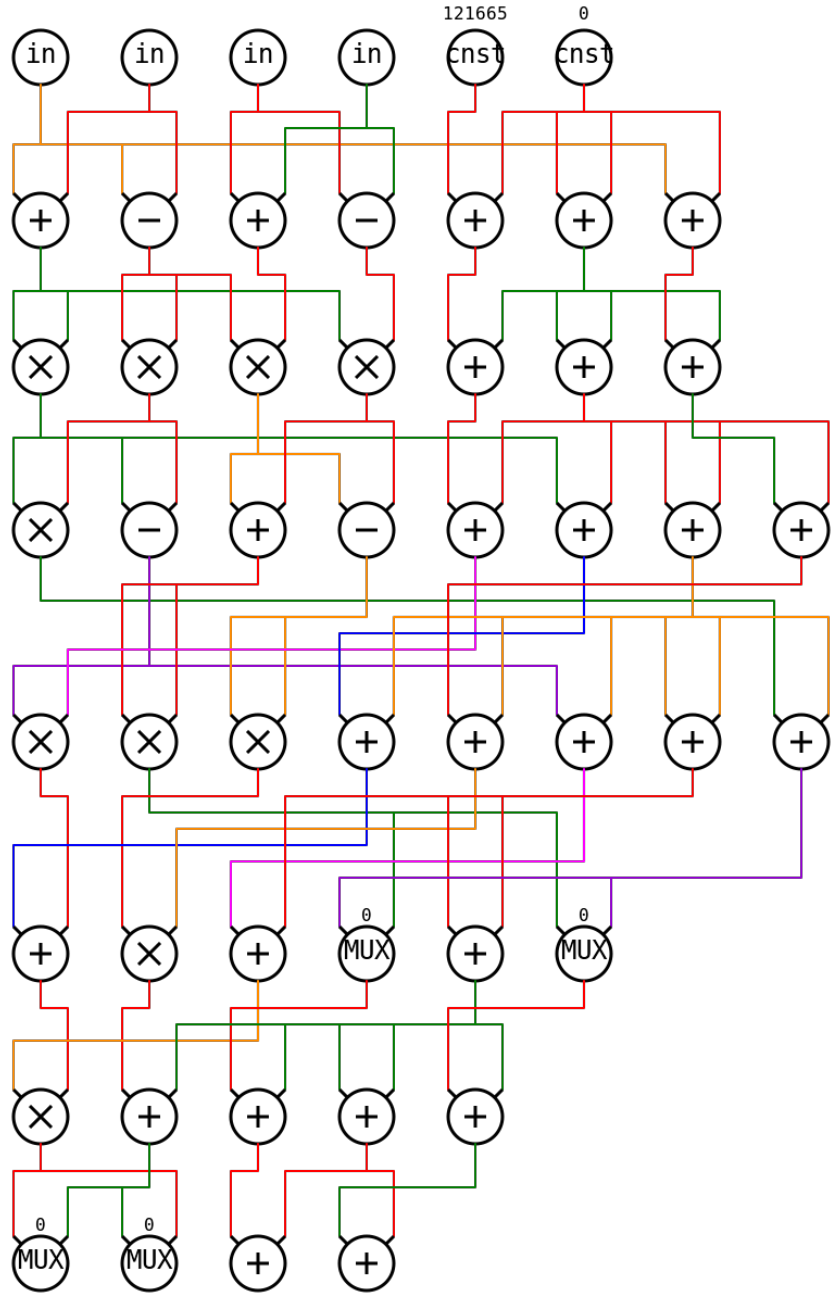

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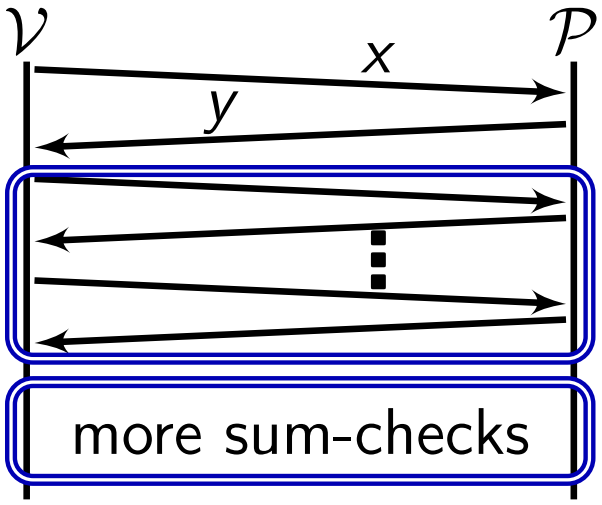
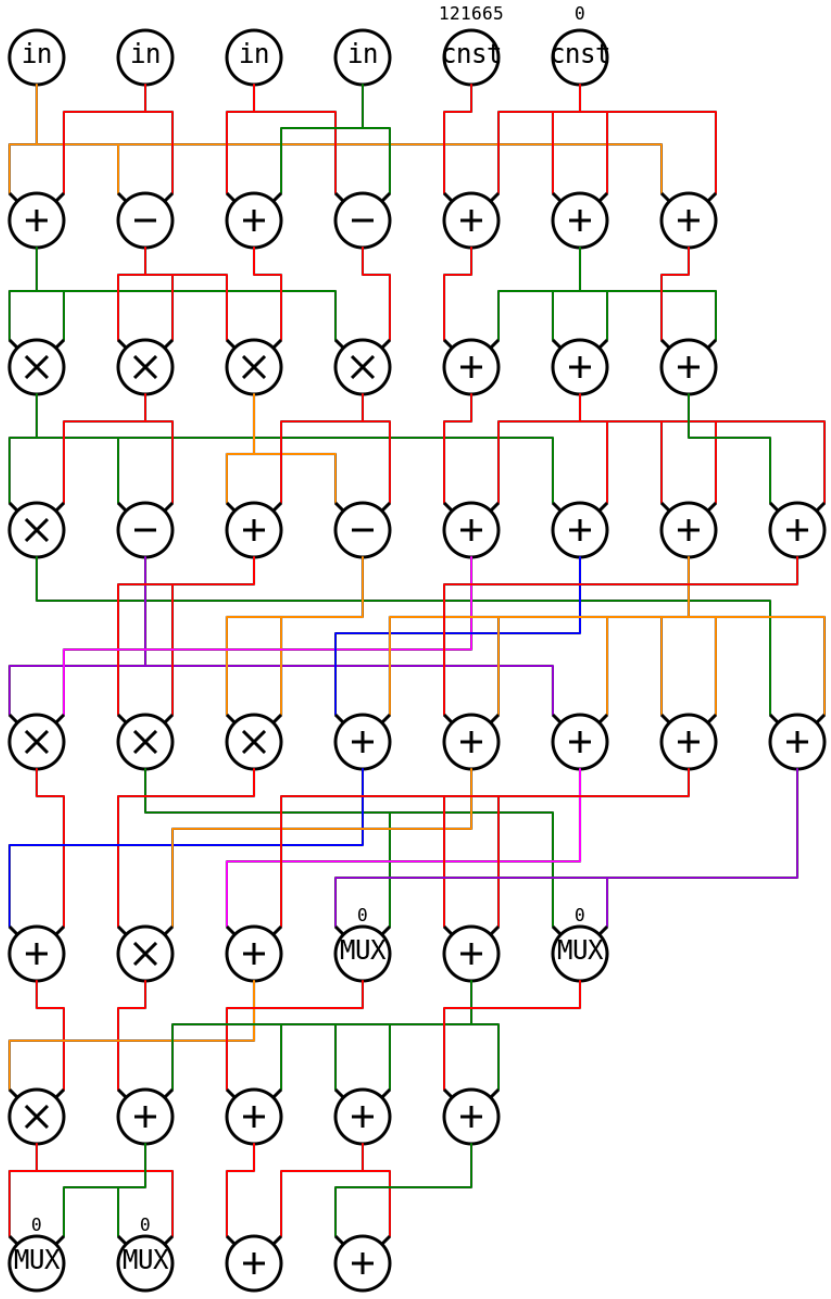
Cost to execute F directly:
O(depth · width)

$\mathcal{V}$'s sequential running time:
O(depth · log width + $|x| + |y|$)
(assuming precomputed queries)



sum-check
[LFKN90]



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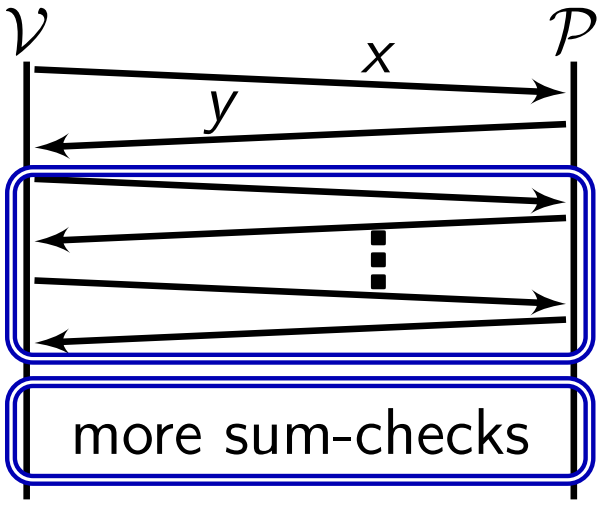
O(depth · width · log width)



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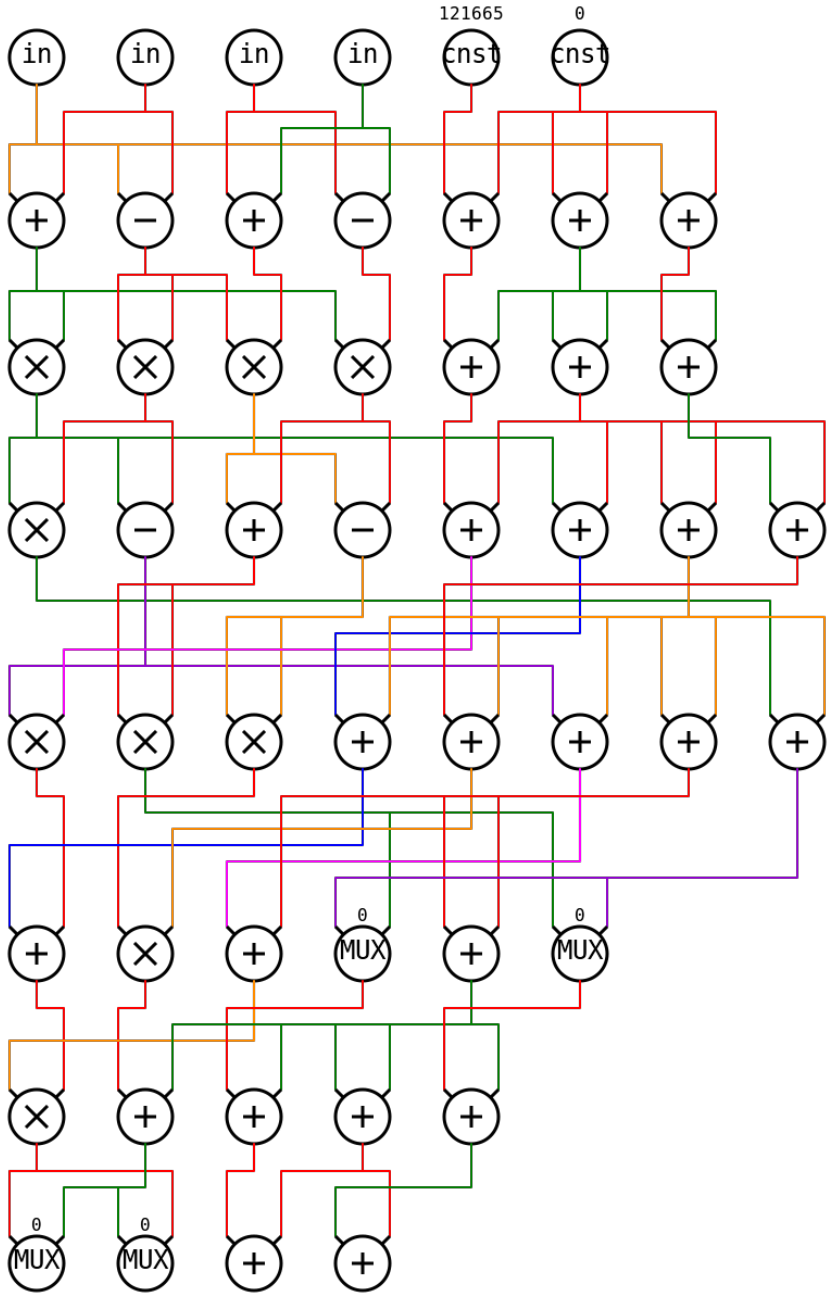
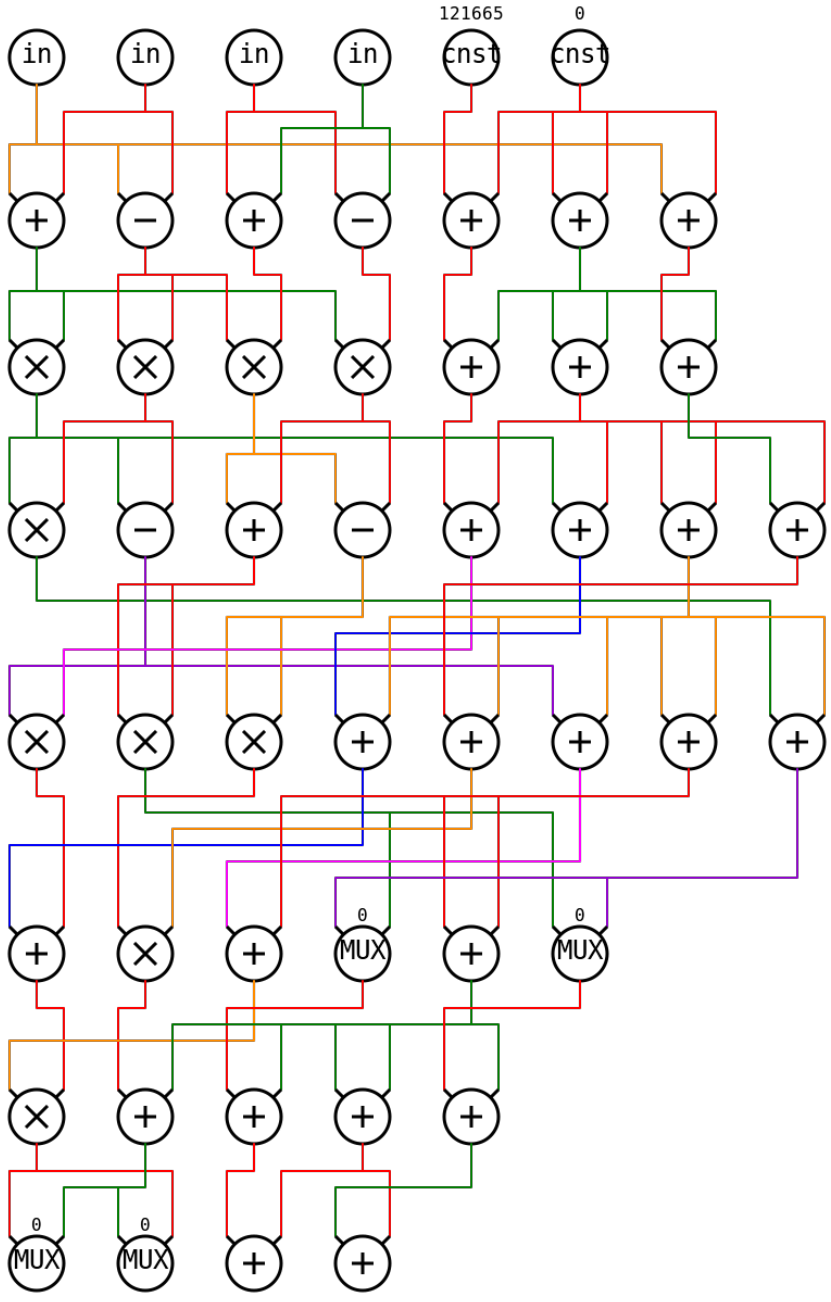
[LFKN90]



Extracting parallelism in Zebra

$\mathcal{P}$ executing AC: layers are sequential, but all gates at a layer can be executed in parallel



Extracting parallelism in Zebra

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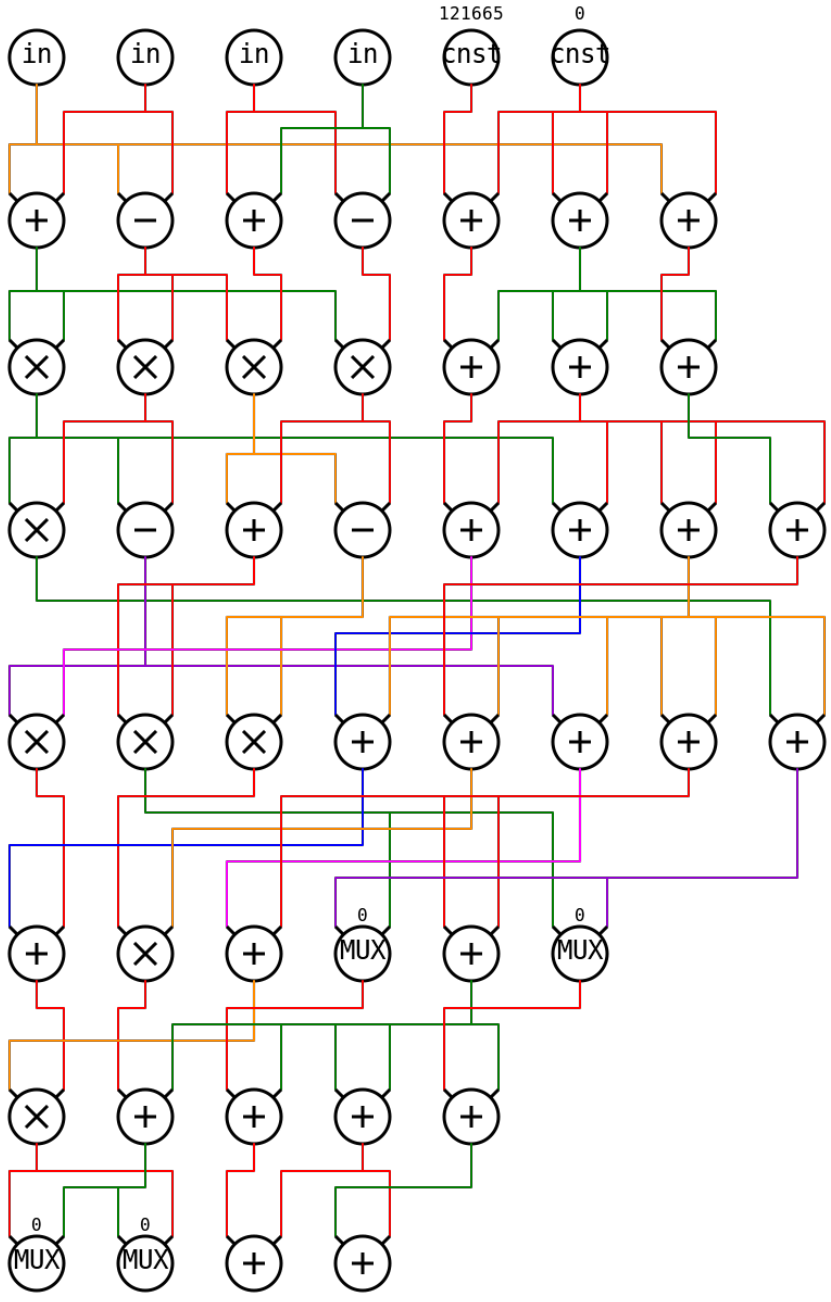
Proving step: Can $\mathcal{V}$ and $\mathcal{P}$ interact about all of F's layers at once?



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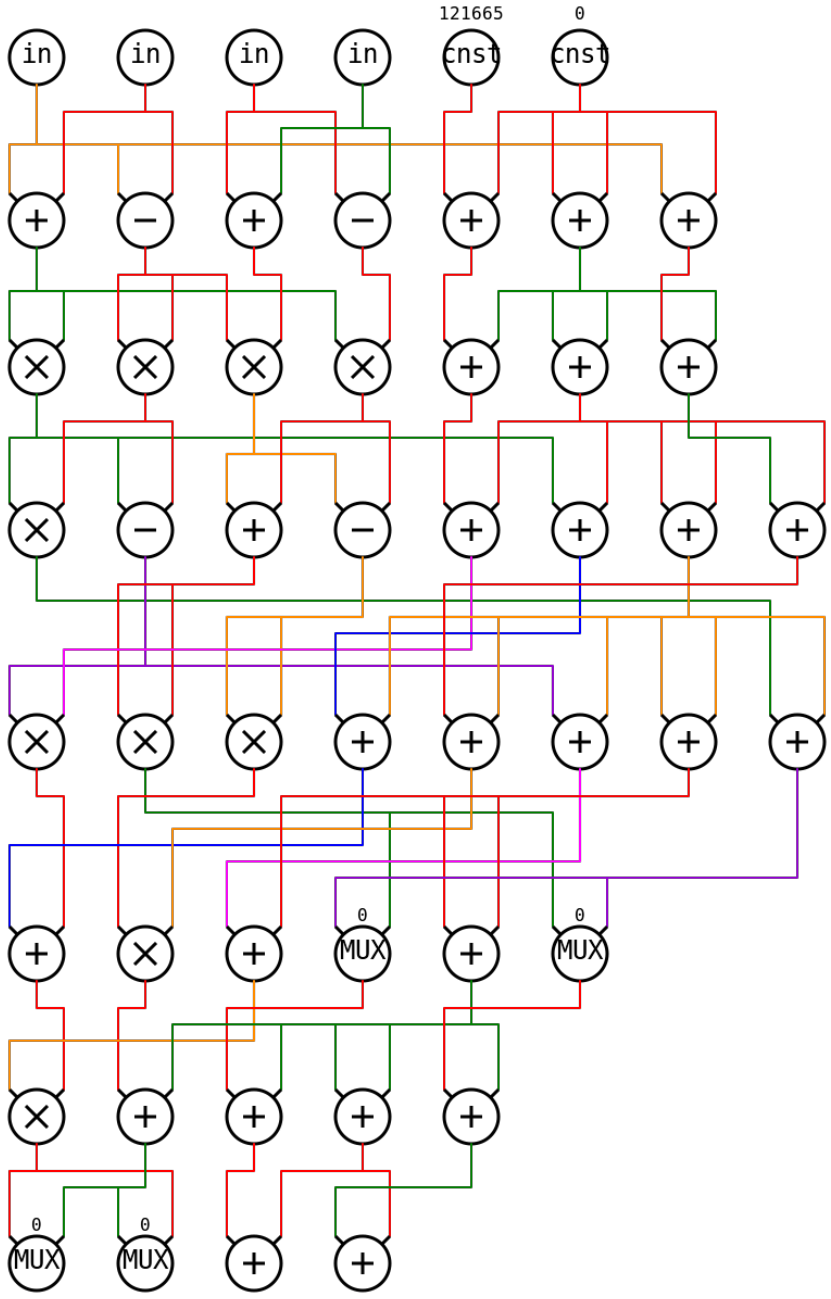

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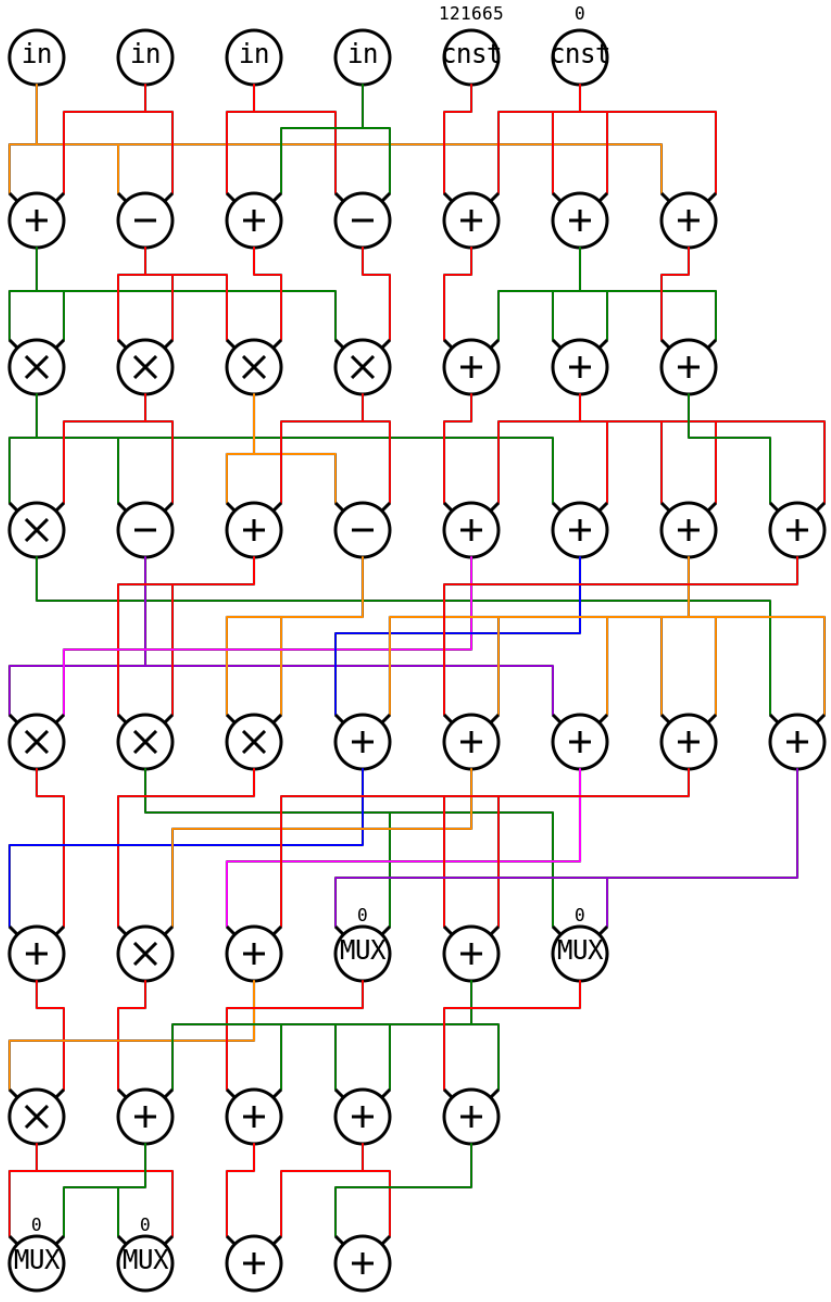
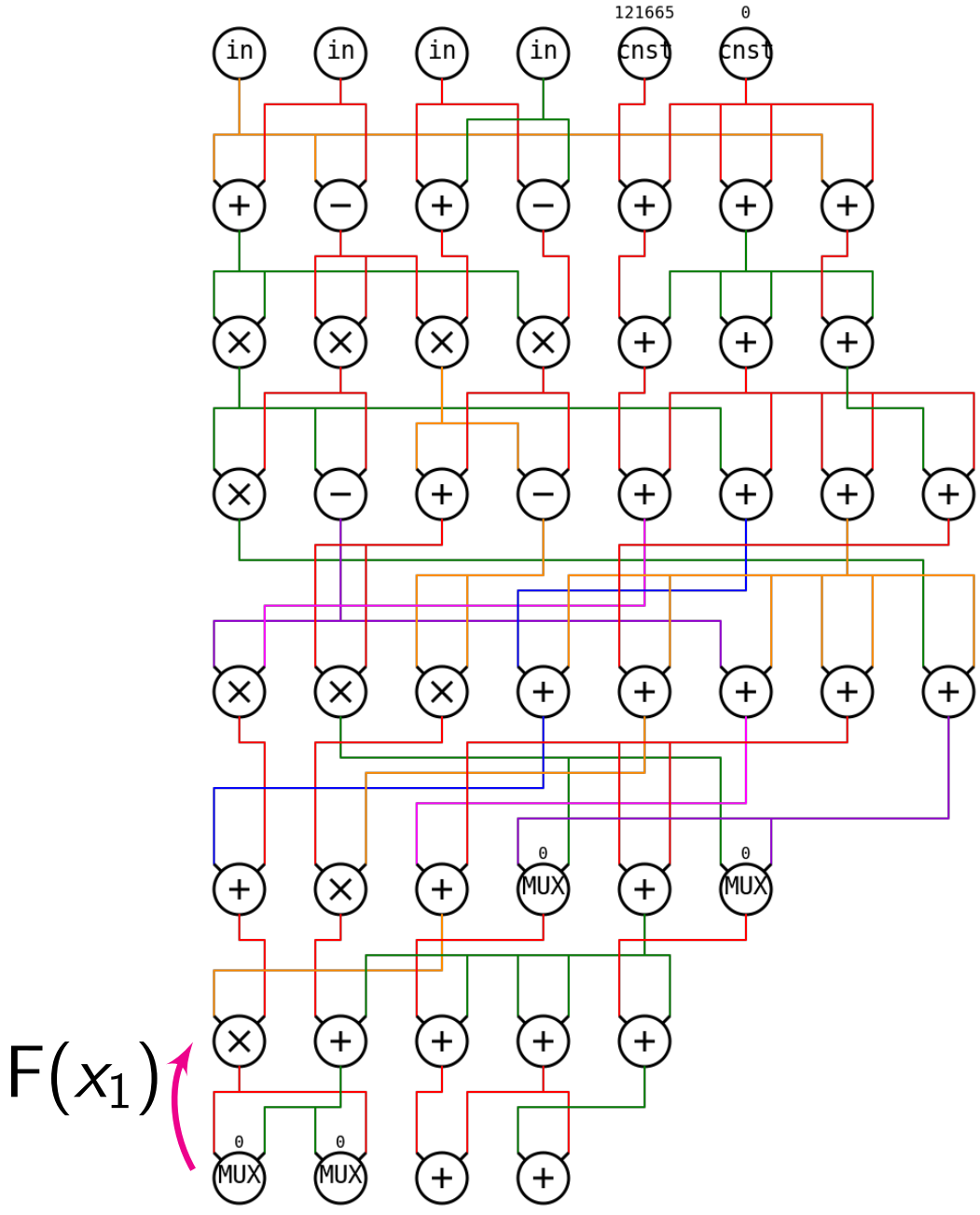
No. $\mathcal{V}$ must ask questions in order or soundness is lost.

But: there is still parallelism to be extracted...



Extracting parallelism in Zebra's $\mathcal{P}$

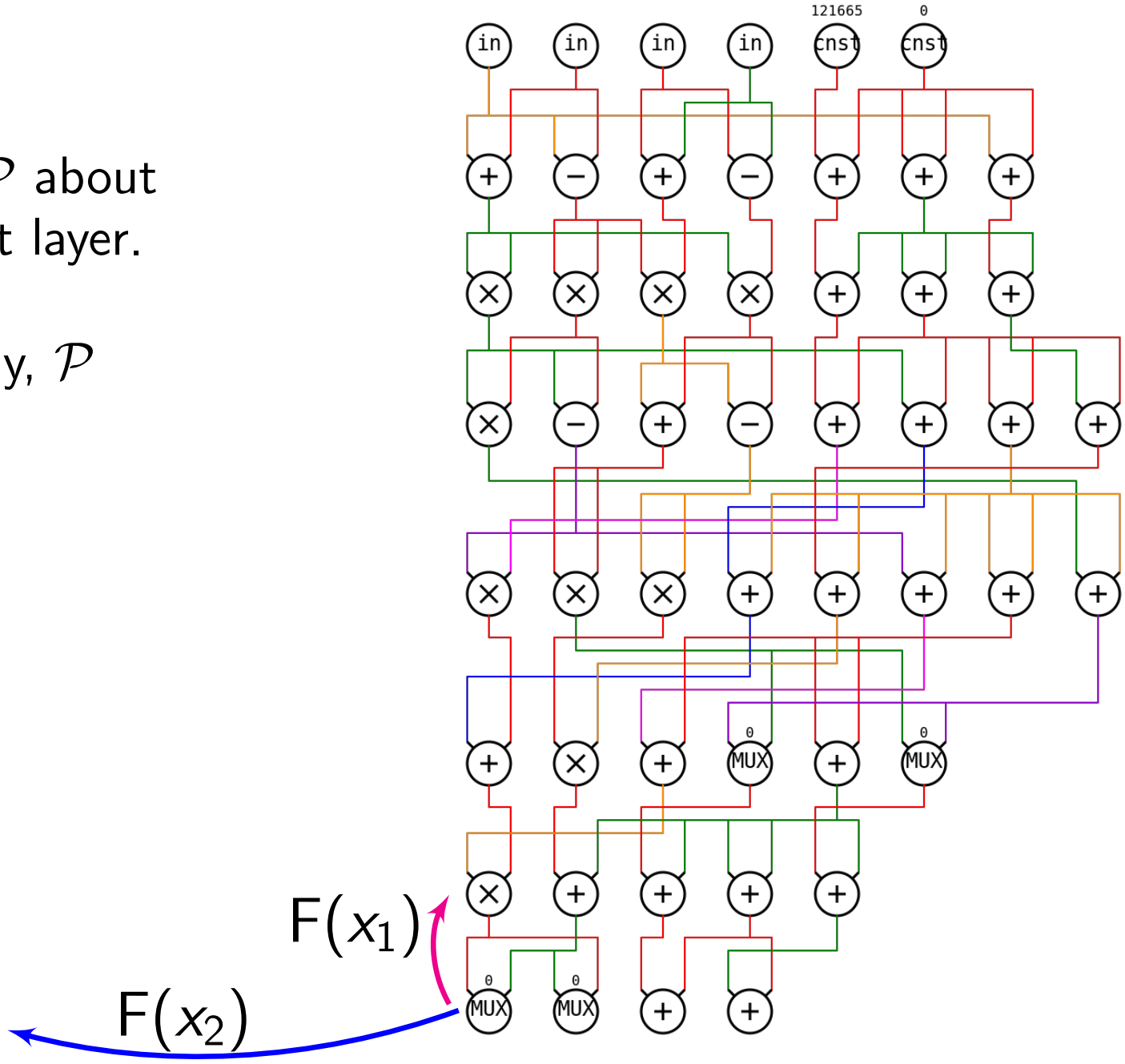
$\mathcal{V}$ questions $\mathcal{P}$ about $\mathsf{F}(x_1)$'s output layer.



Extracting parallelism in Zebra's $\mathcal{P}$

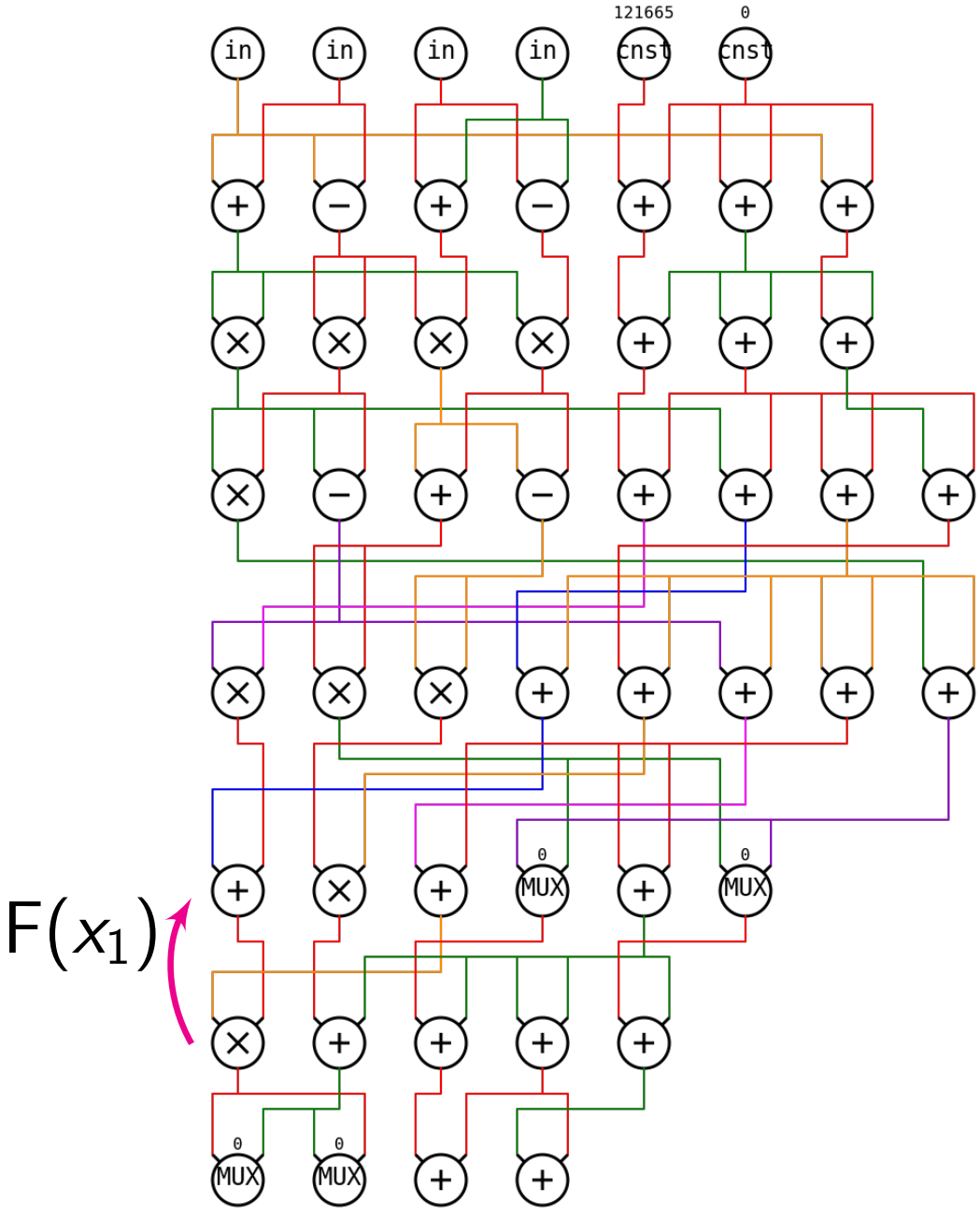
$\mathcal{V}$ questions $\mathcal{P}$ about $\mathsf{F}(x_1)$'s output layer.

Simultaneously, $\mathcal{P}$ returns $\mathsf{F}(x_2)$.



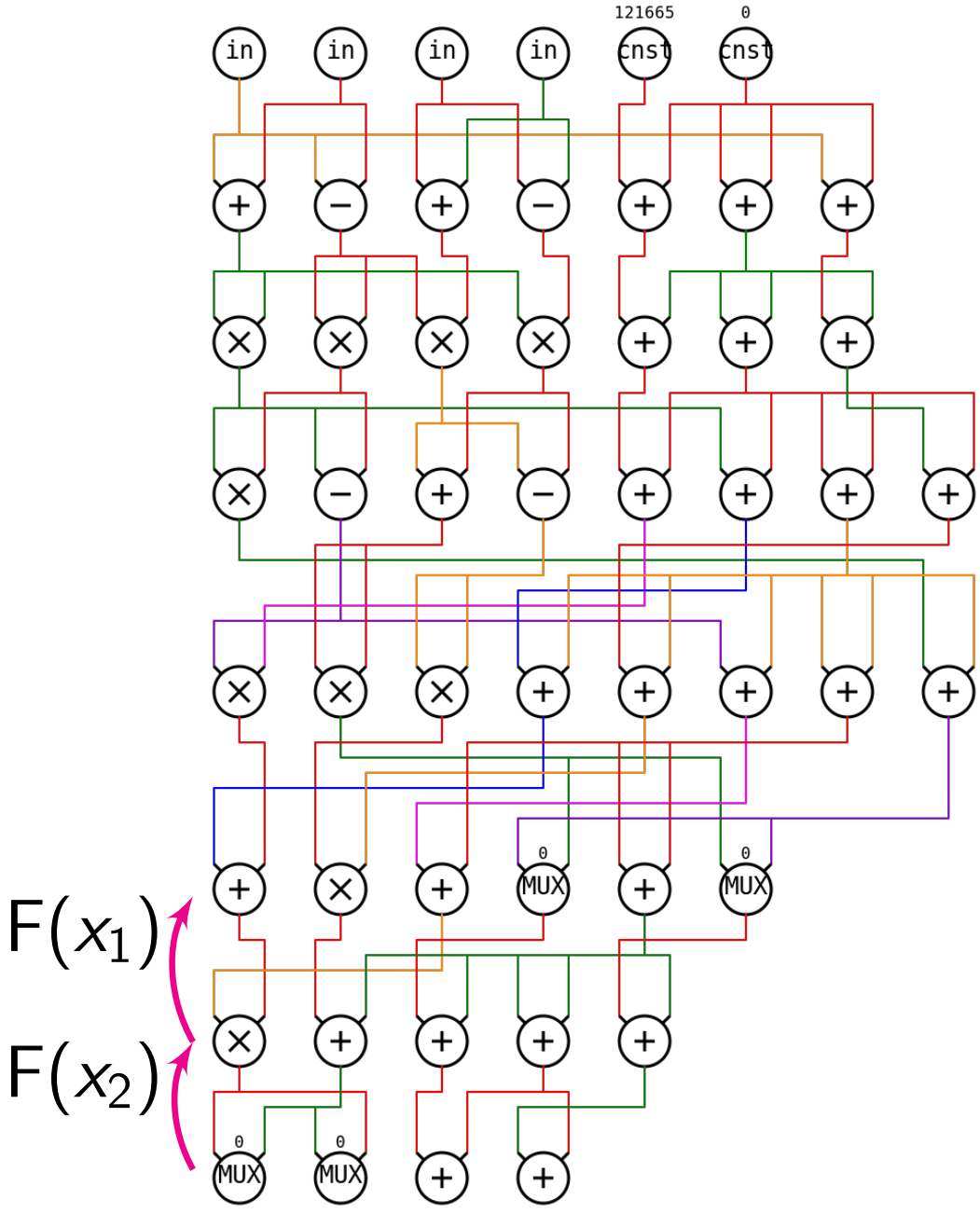
Extracting parallelism in Zebra's $\mathcal{P}$

$\mathcal{V}$ questions $\mathcal{P}$ about
$\mathsf{F}(x_1)$'s next layer



Extracting parallelism in Zebra's $\mathcal{P}$

$\mathcal{V}$ questions $\mathcal{P}$ about
$\mathsf{F}(x_1)$'s next layer, and
$\mathsf{F}(x_2)$'s output layer.



Extracting parallelism in Zebra's $\mathcal{P}$

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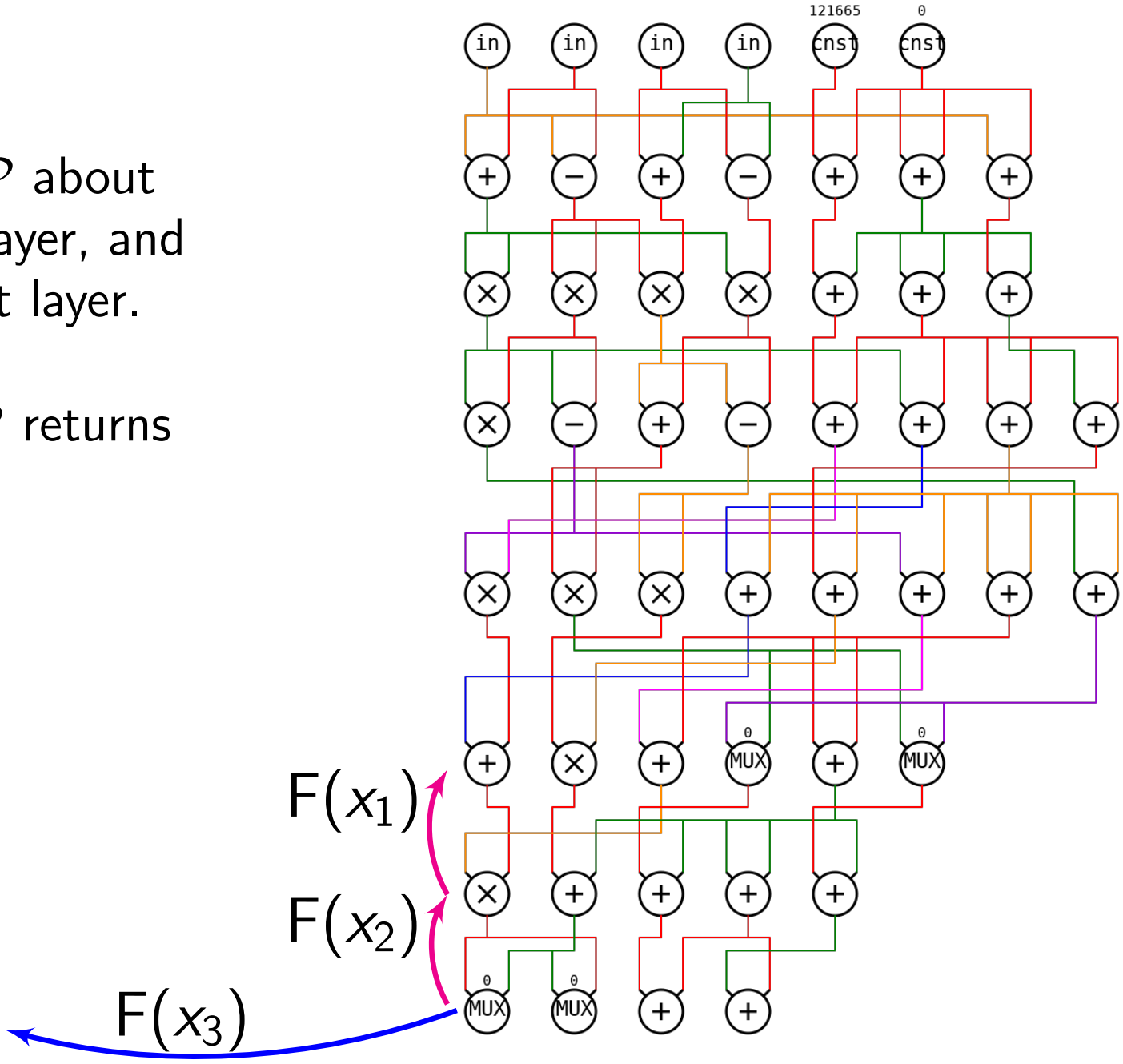
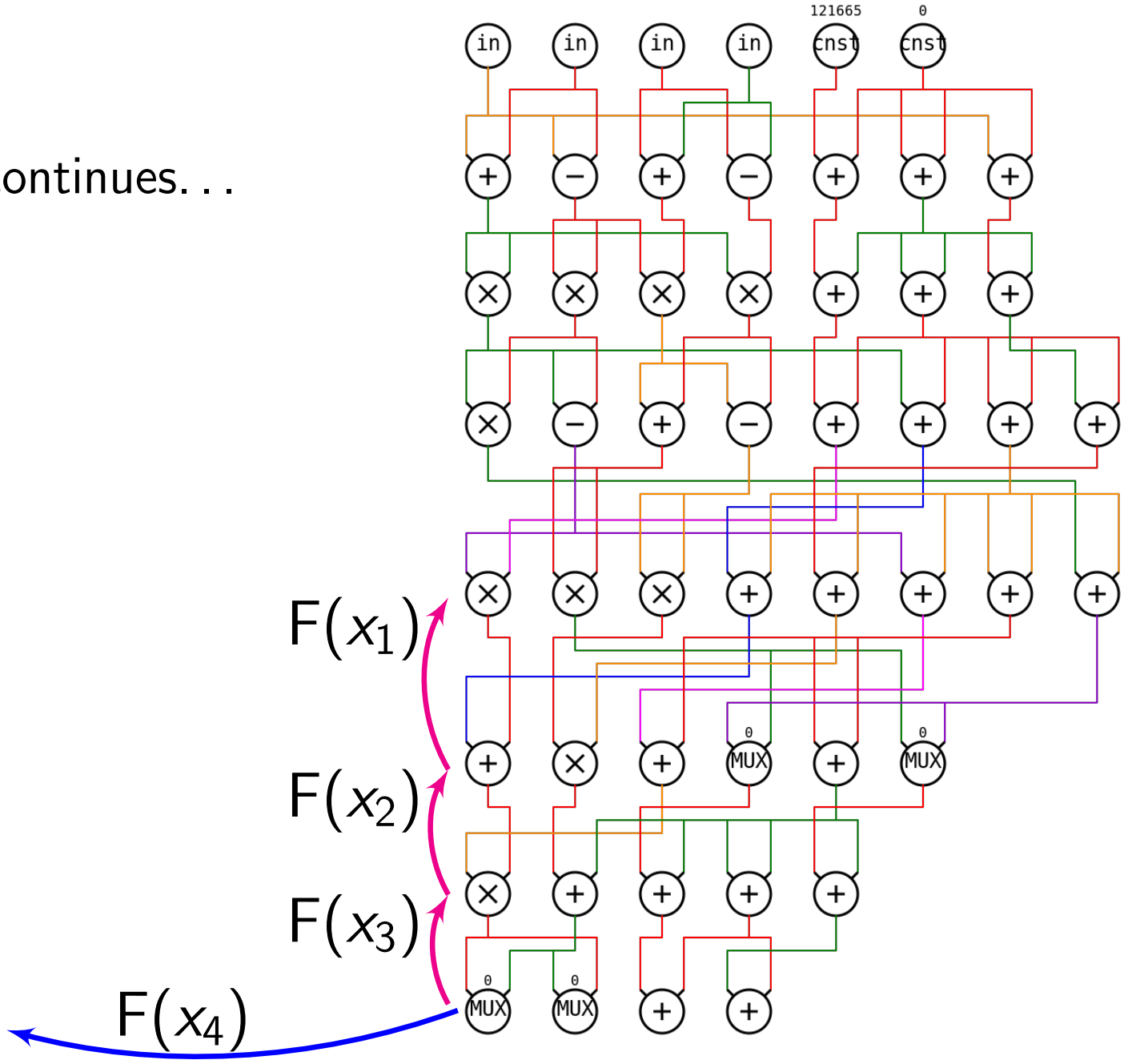
Meanwhile, $\mathcal{P}$ returns $\mathsf{F}(x_3)$.



Extracting parallelism in Zebra's $\mathcal{P}$

This process continues...



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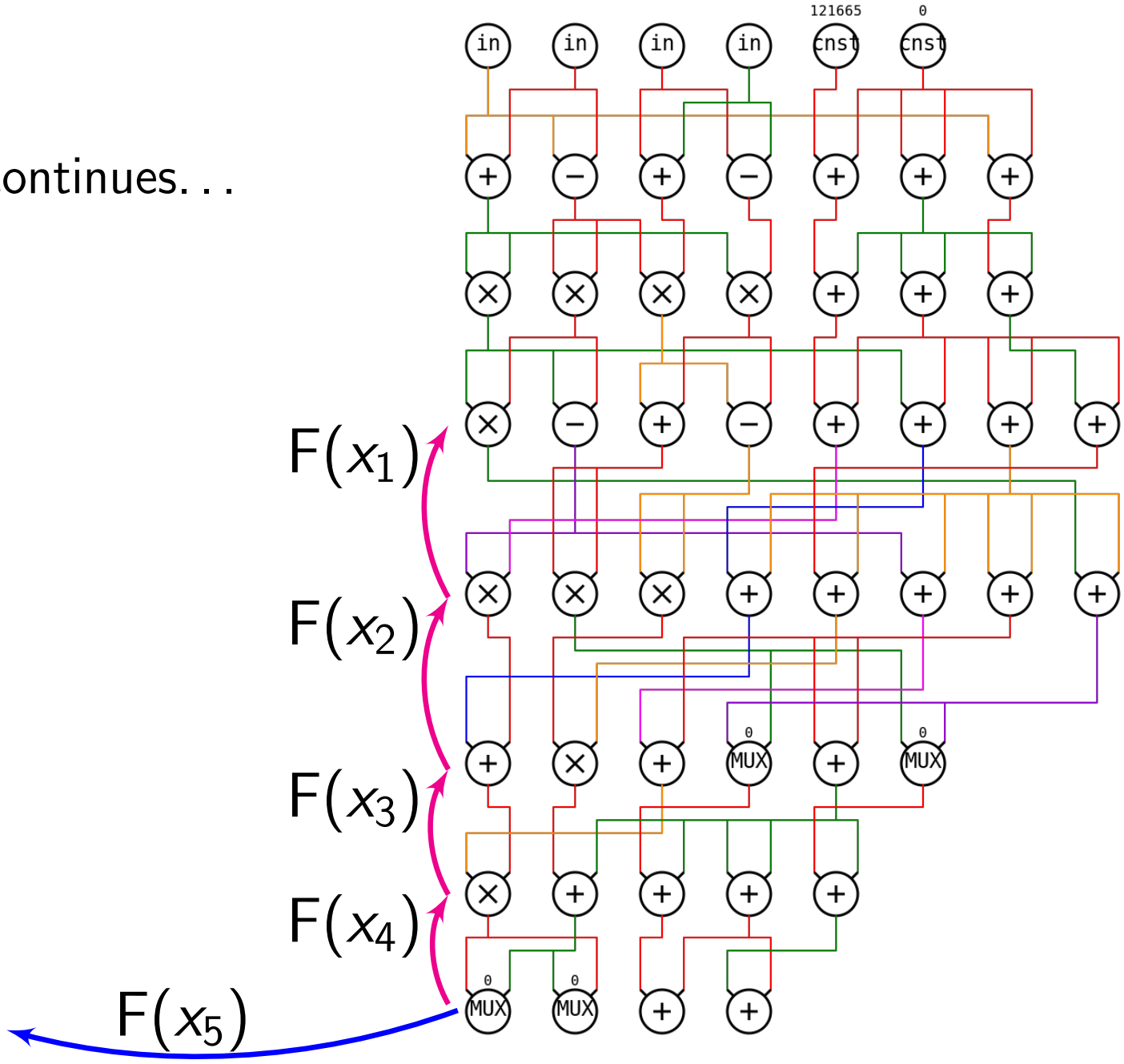
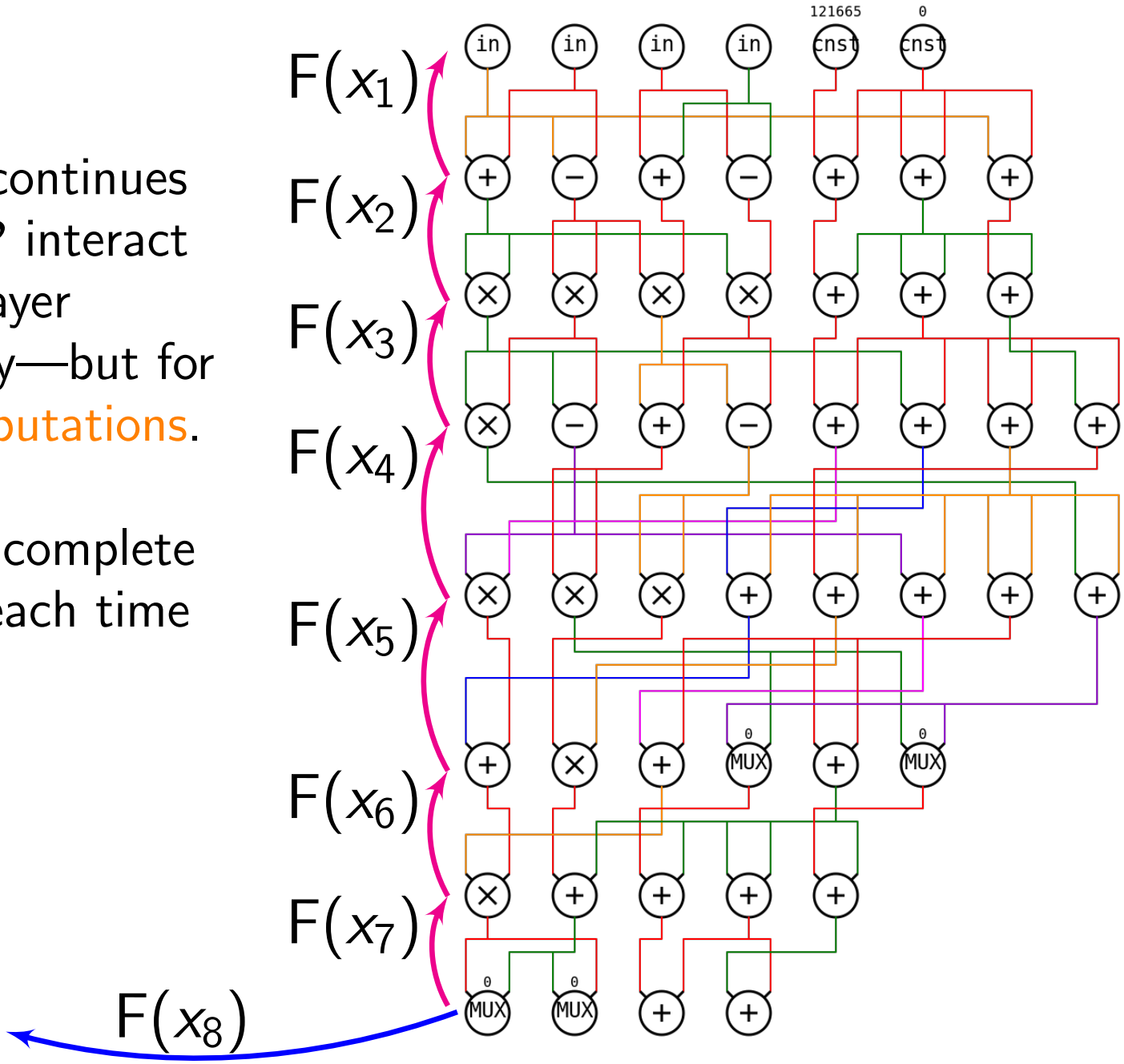


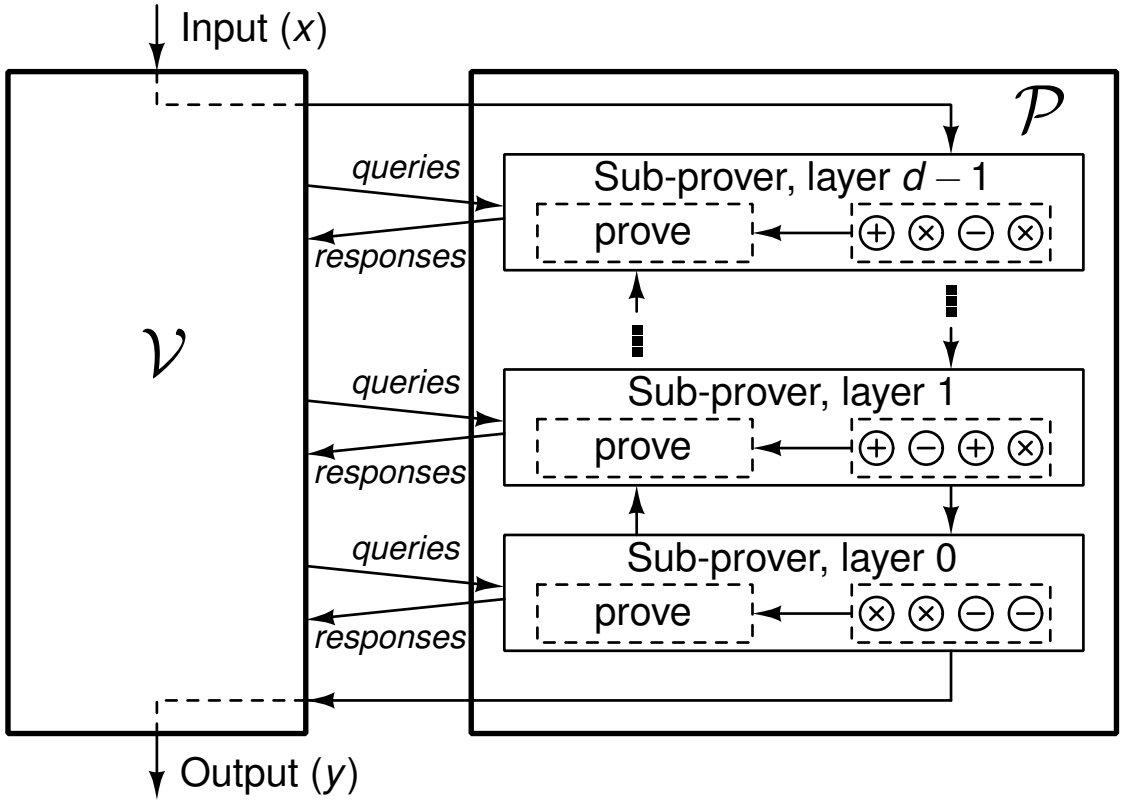
Extracting parallelism in Zebra's $\mathcal{P}$

This process continues until $\mathcal{V}$ and $\mathcal{P}$ interact about every layer simultaneously—but for different computations.

$\mathcal{V}$ and $\mathcal{P}$ can complete one proof in each time step.

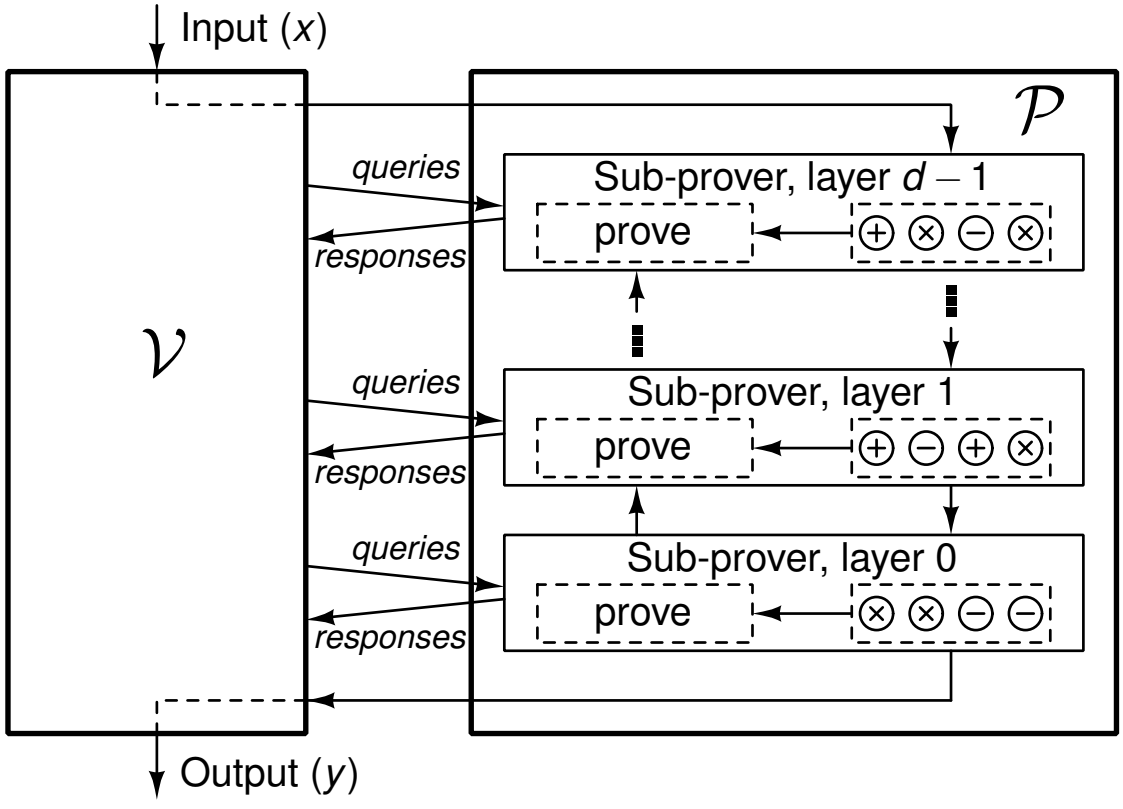


Extracting parallelism in Zebra's $\mathcal{P}$ with pipelining



This approach is just a standard hardware technique, pipelining; it is possible because the protocol is naturally staged.

Extracting parallelism in Zebra's $\mathcal{P}$ with pipelining

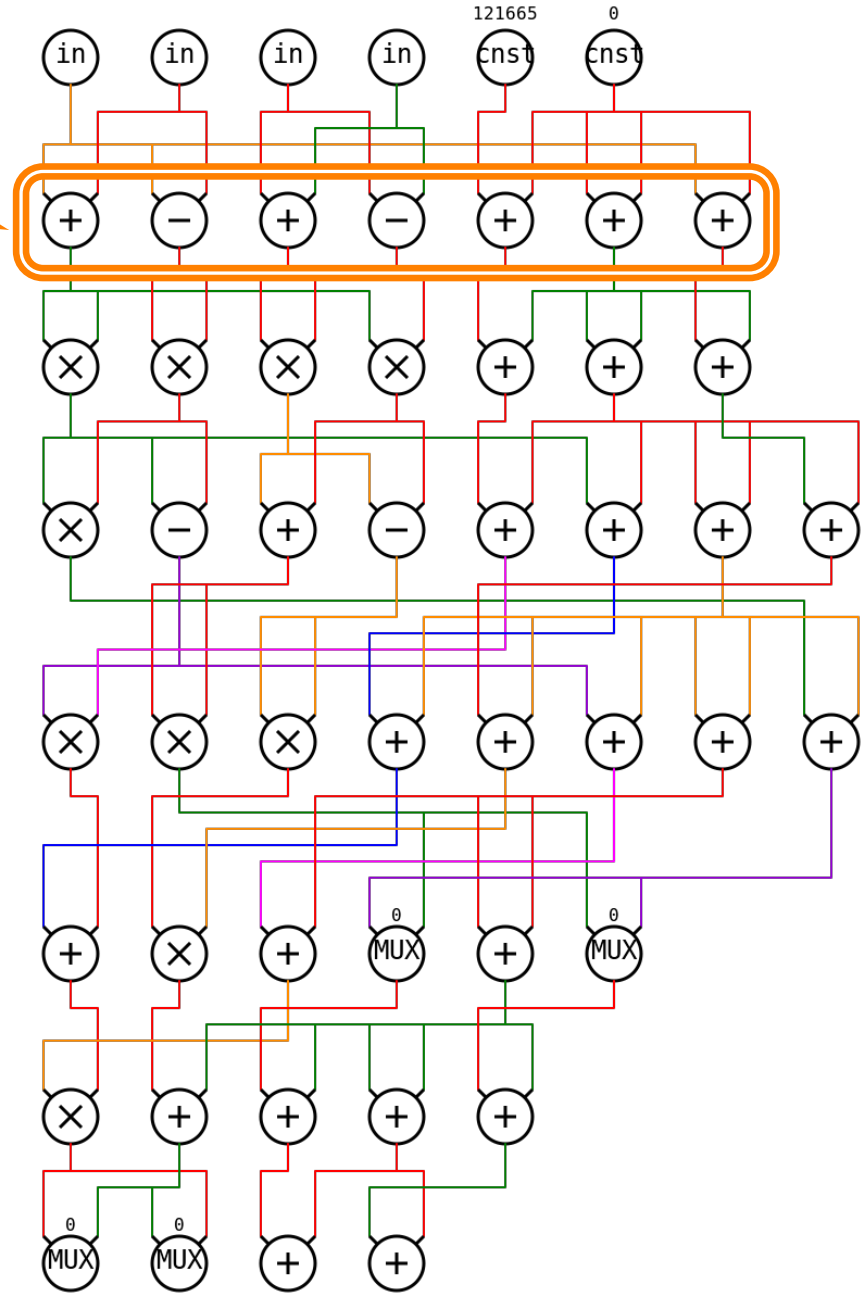


This approach is just a standard hardware technique, pipelining; it is possible because the protocol is naturally staged.

There are other opportunities to leverage the protocol's structure.

Per-layer computations

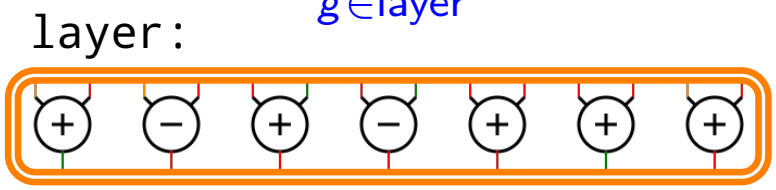
For each sum-check round, $\mathcal{P}$ sums over each gate in a layer



Per-layer computations

For each sum-check round, $\mathcal{P}$ sums over each gate in a layer, evaluating $\mathrm{H}[k]$, $k \in \{0, 1, 2\}$

$$\mathrm{H}[k] = \sum_{g \in \text{layer}} \delta(g, k)$$



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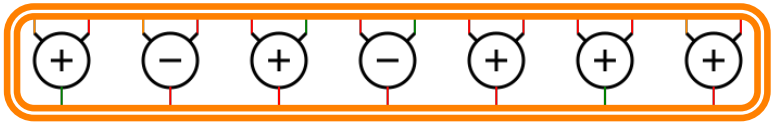
layer:



In software:

```
// compute H[0],H[1],H[2]
for k ∈ {0, 1, 2}:
  H[k] ← 0
  for g ∈ layer:
    H[k] ← H[k] + δ(g, k)
    // δ uses state[g]

// update lookup table
// with 𝒱's random coin
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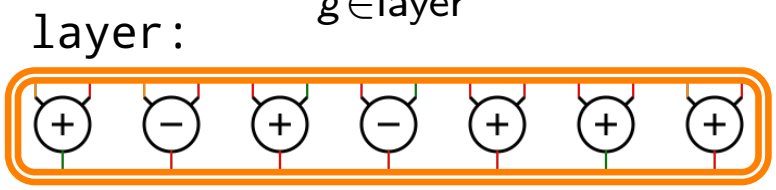

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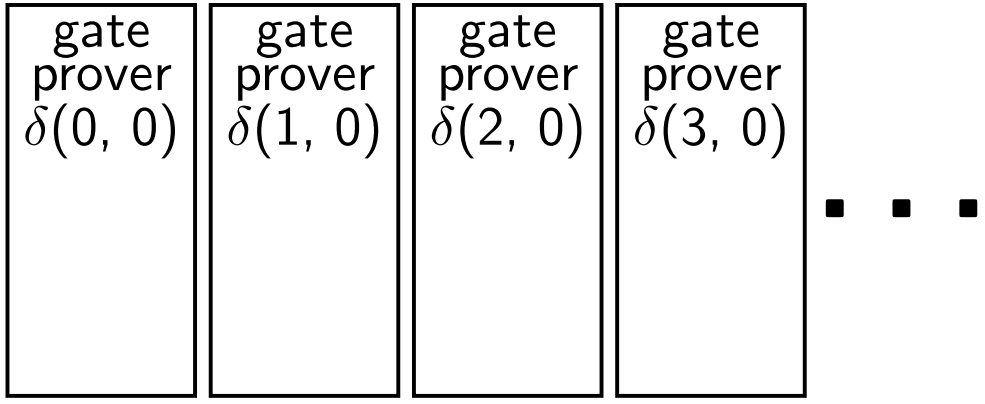

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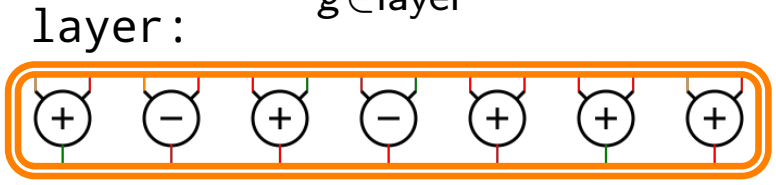

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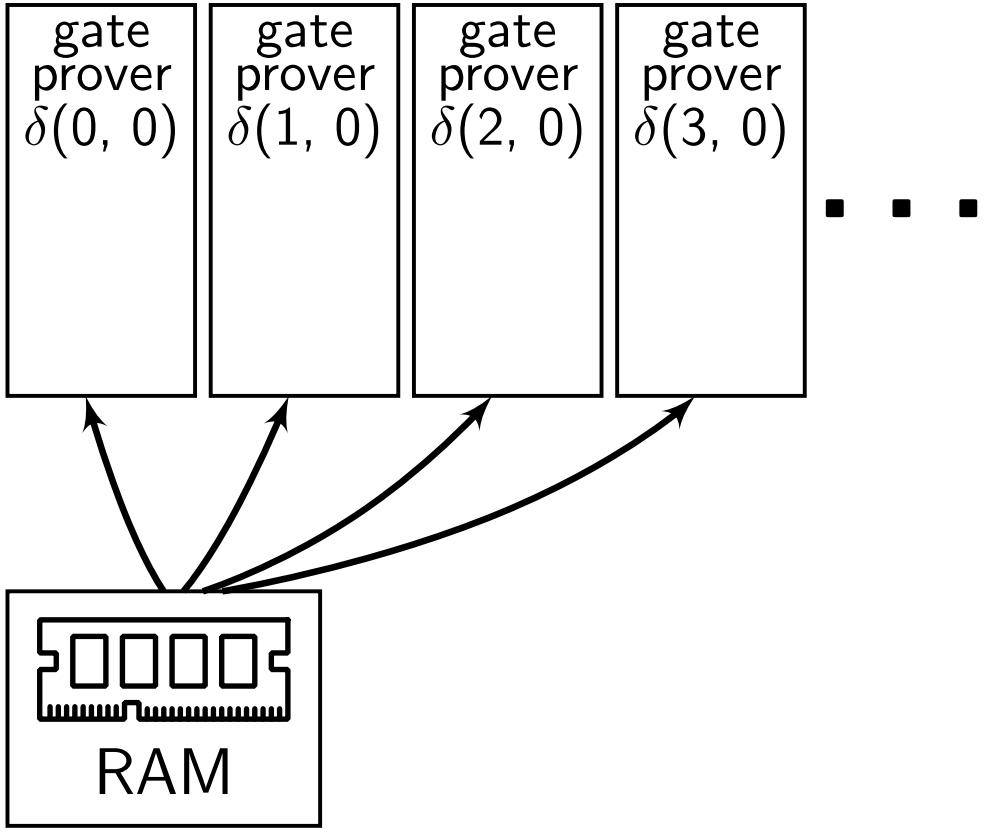

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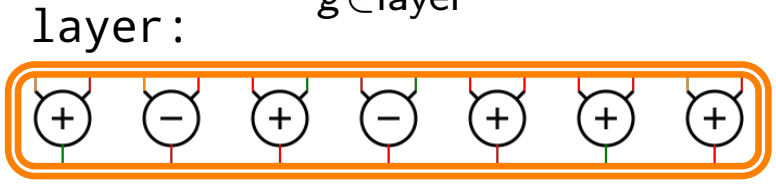

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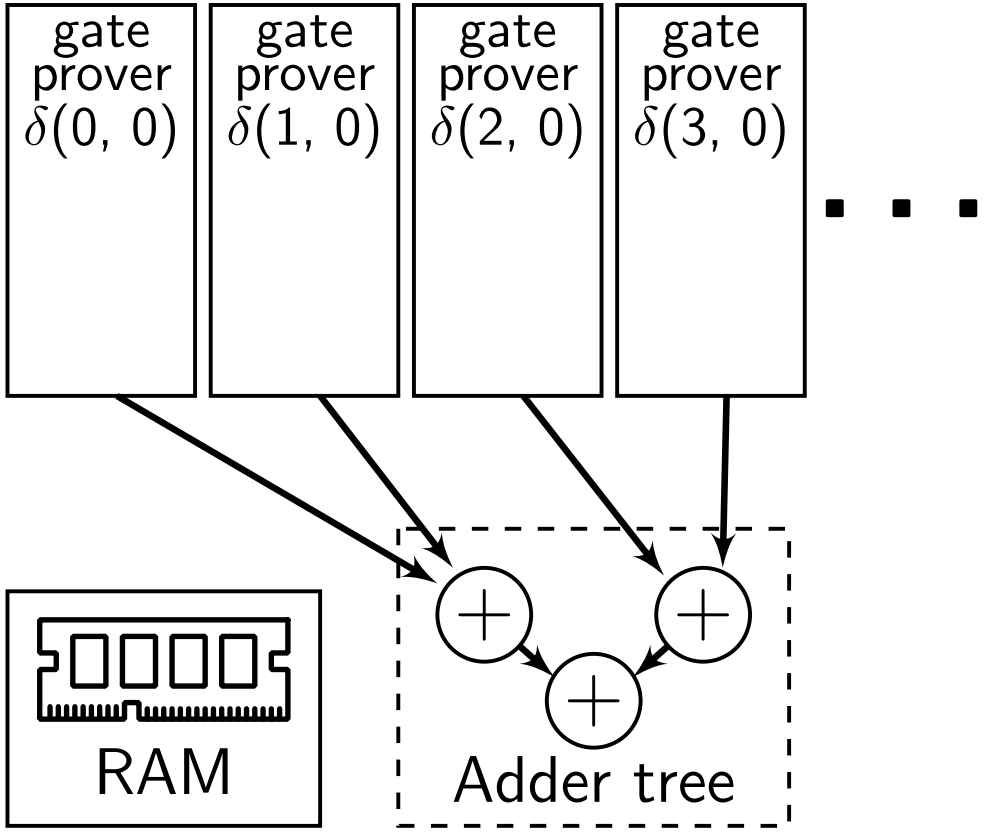

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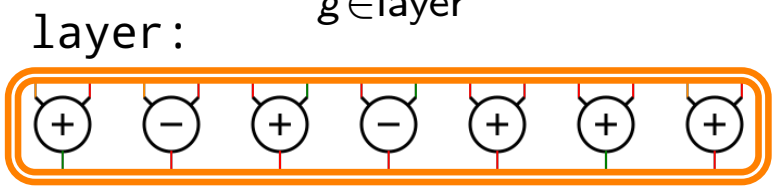

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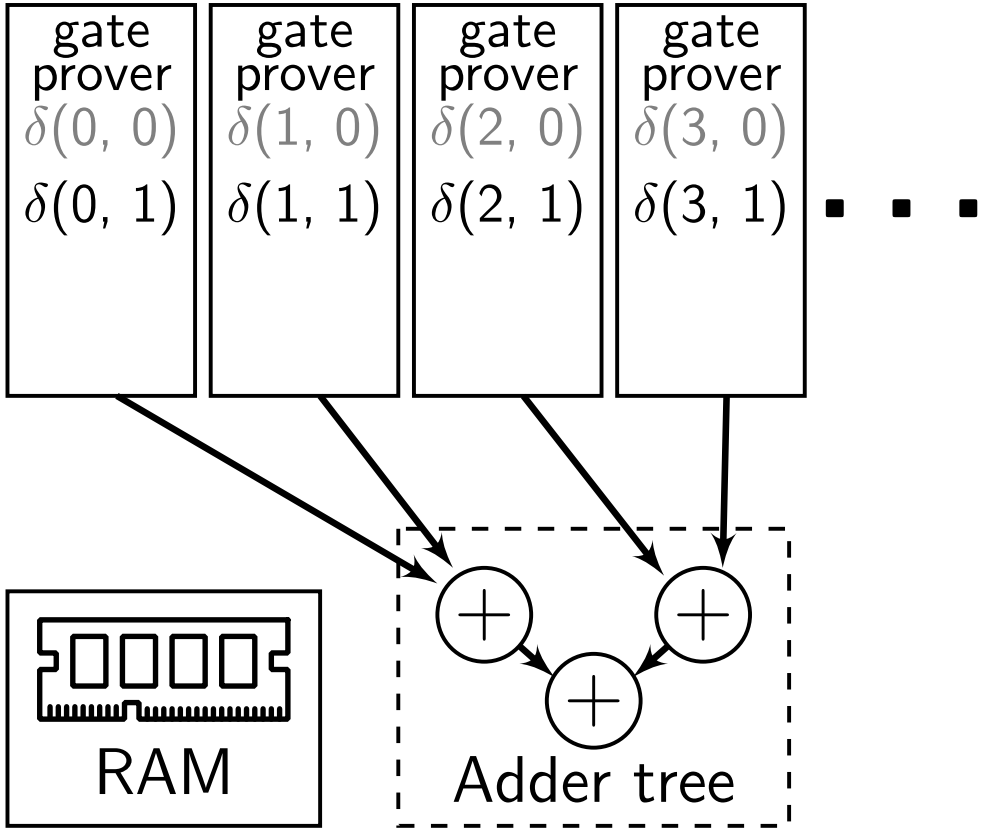

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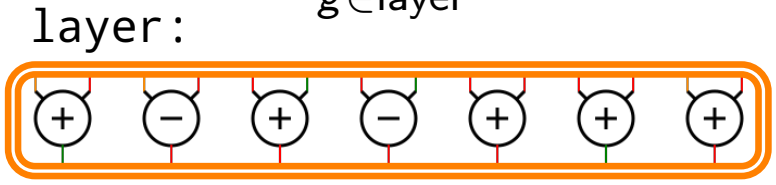

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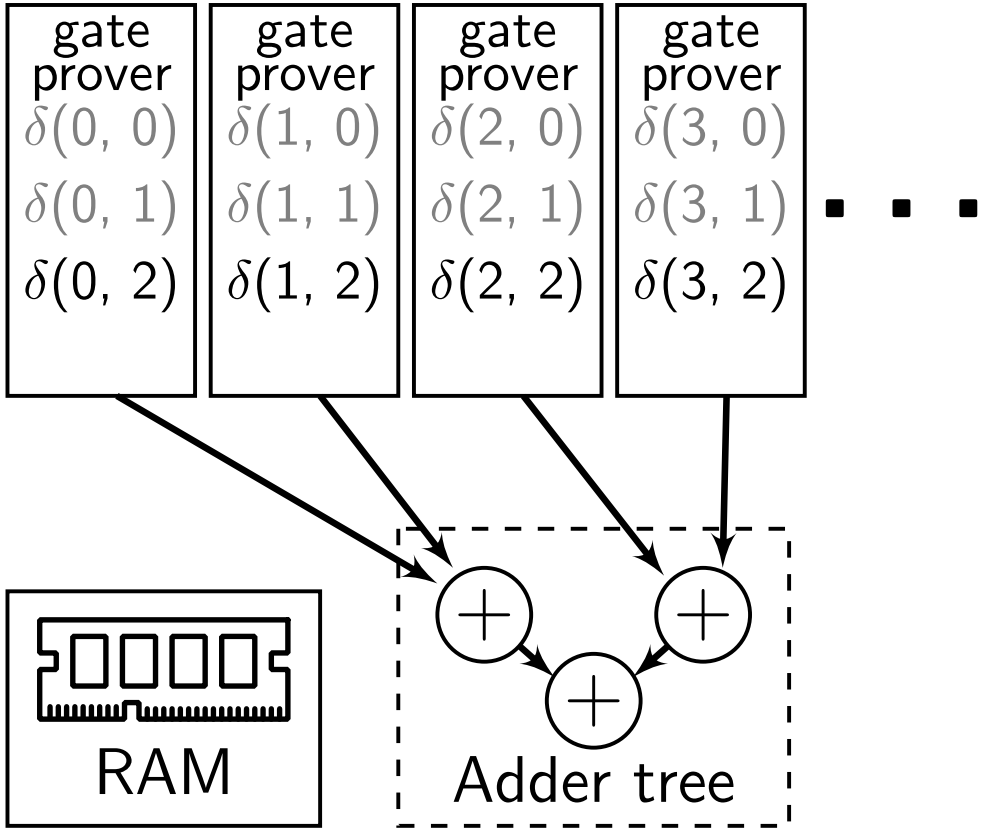

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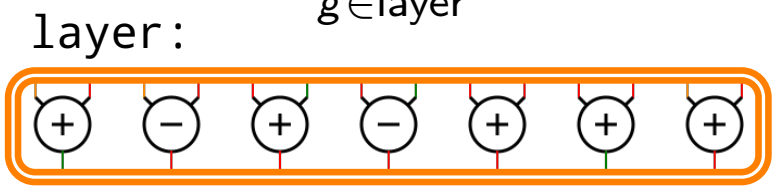

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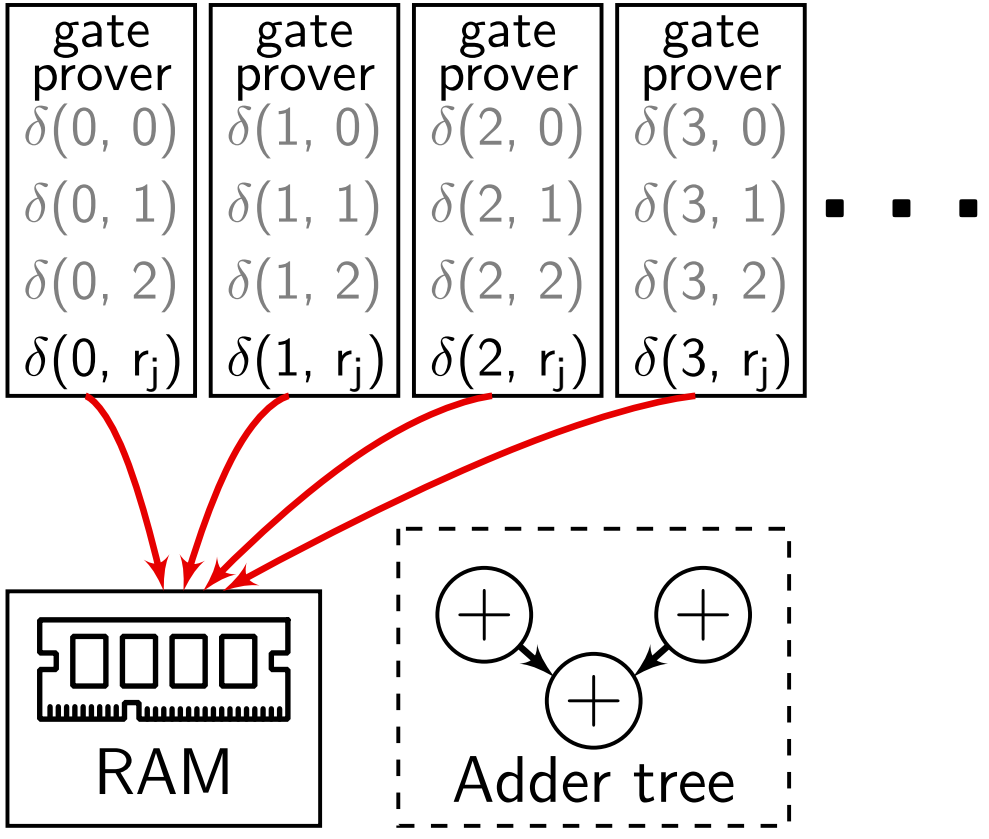

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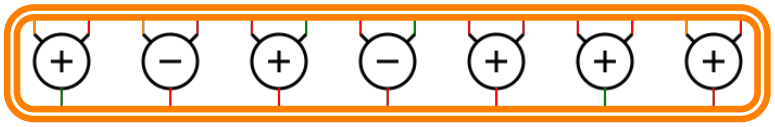

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In hardware:

gate prover	gate prover	gate prover	gate prover
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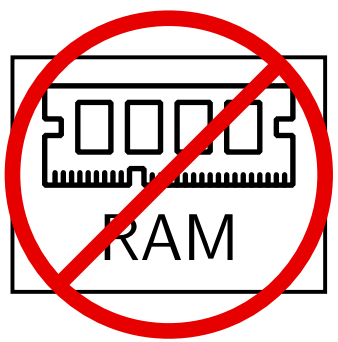
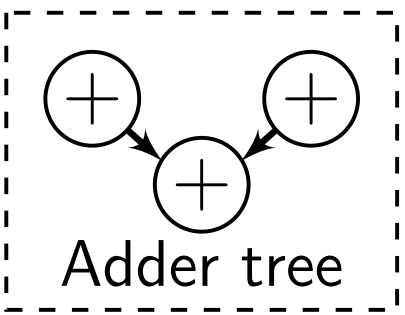
$\delta(0, 1)$	$\delta(1, 1)$	$\delta(2, 1)$	$\delta(3, 1)$
$\delta(0, 2)$	$\delta(1, 2)$	$\delta(2, 2)$	$\delta(3, 2)$
$\delta(0, r_j)$	$\delta(1, r_j)$	$\delta(2, r_j)$	$\delta(3, r_j)$





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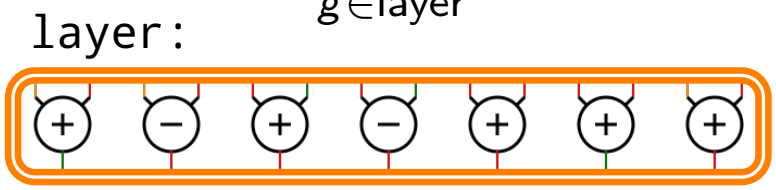

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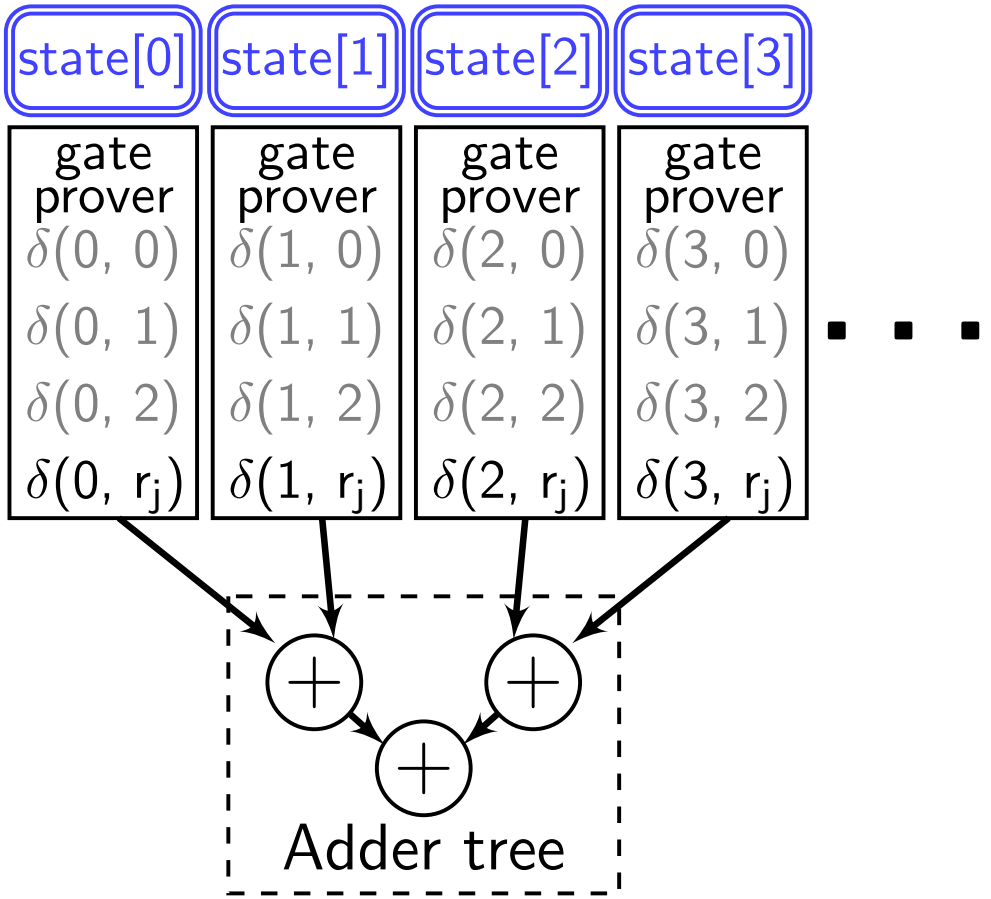

Zebra's design approach

✓ Extract parallelism

e.g., pipelined proving
e.g., parallel evaluation of δ by gate provers

✓ Exploit locality: distribute data and control

e.g., no RAM: data is kept close to places it is needed

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✓ Reduce, reuse, recycle

e.g., computation: save energy by adding memoization to $\mathcal{P}$
e.g., hardware: save chip area by reusing the same circuits

Architectural challenges

Interaction between $\mathcal{V}$ and $\mathcal{P}$ requires a lot of bandwidth

✗ $\mathcal{V}$ and $\mathcal{P}$ on circuit board? Too much energy, circuit area

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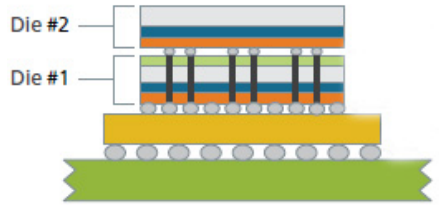

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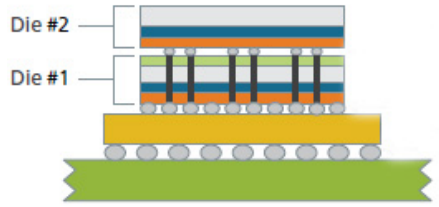

Protocol requires input-independent precomputation [VSBW13]

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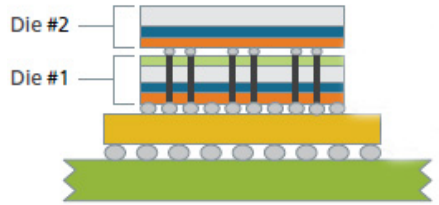

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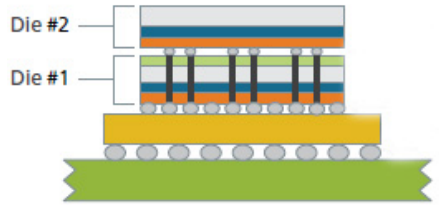

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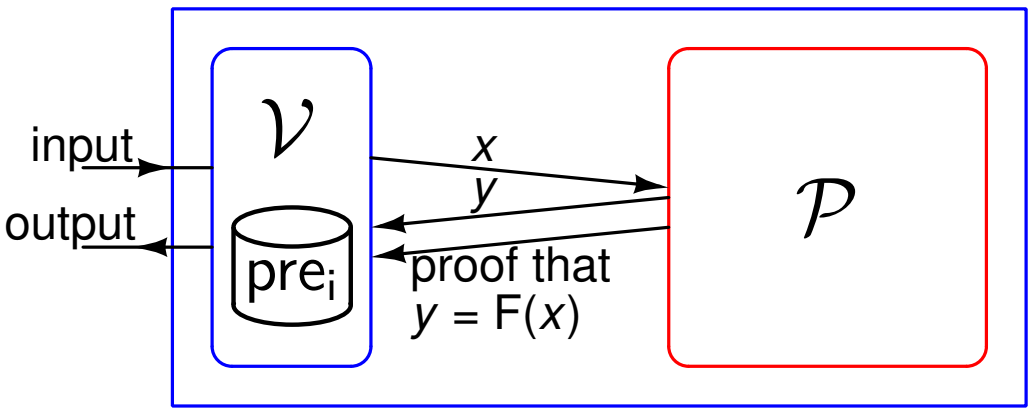

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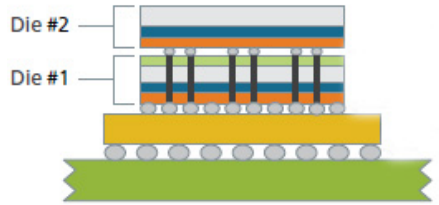

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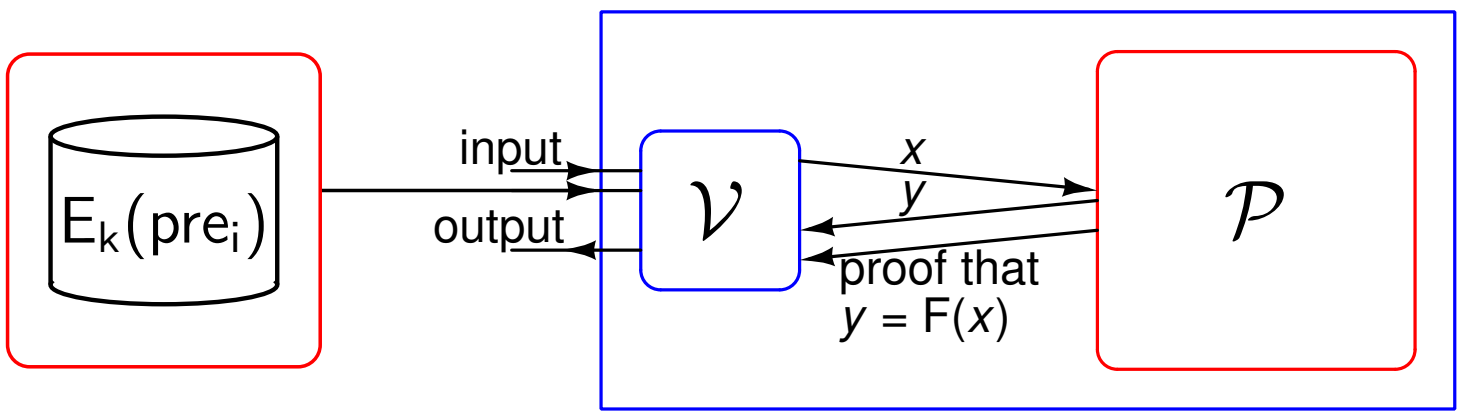

Implementation

Zebra's implementation includes

- a compiler that produces synthesizable Verilog for $\mathcal{P}$
- two $\mathcal{V}$ implementations
  - hardware (Verilog)
  - software (C++)
- library to generate $\mathcal{V}$'s precomputations
- Verilog simulator extensions to model software or hardware $\mathcal{V}$'s interactions with $\mathcal{P}$

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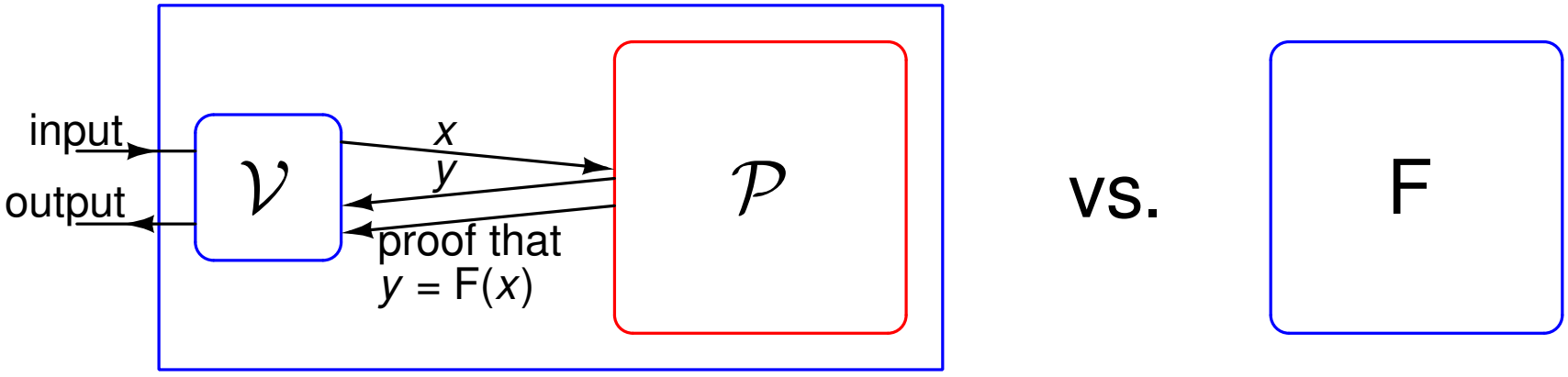
Evaluation method



Baseline: direct implementation of F in same technology as $\mathcal{V}$

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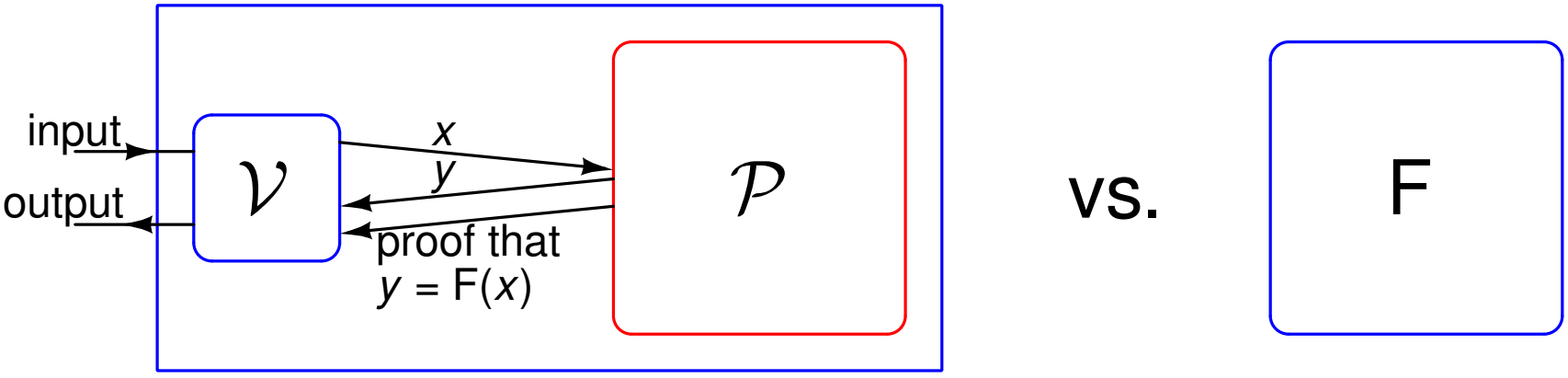

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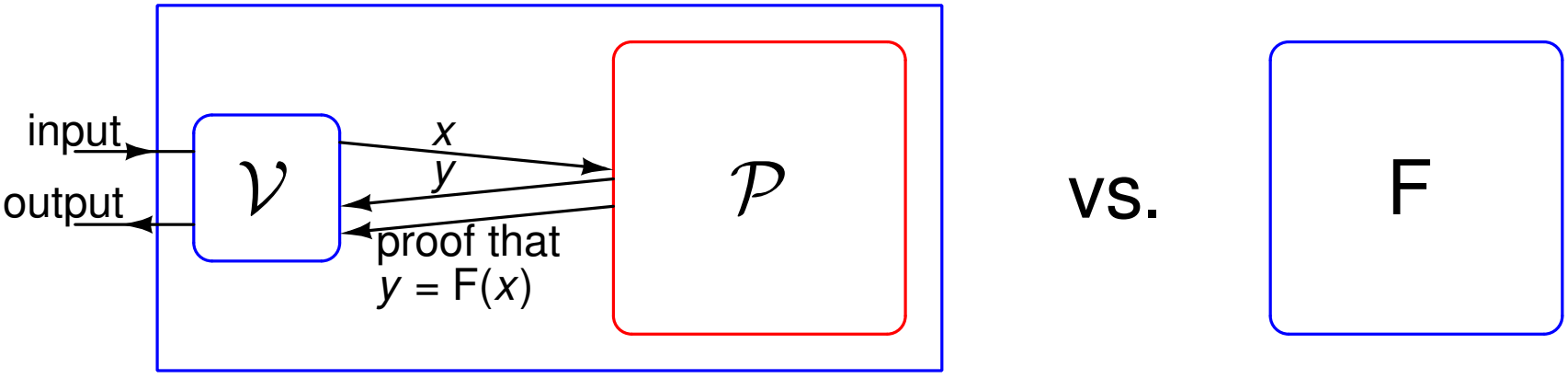

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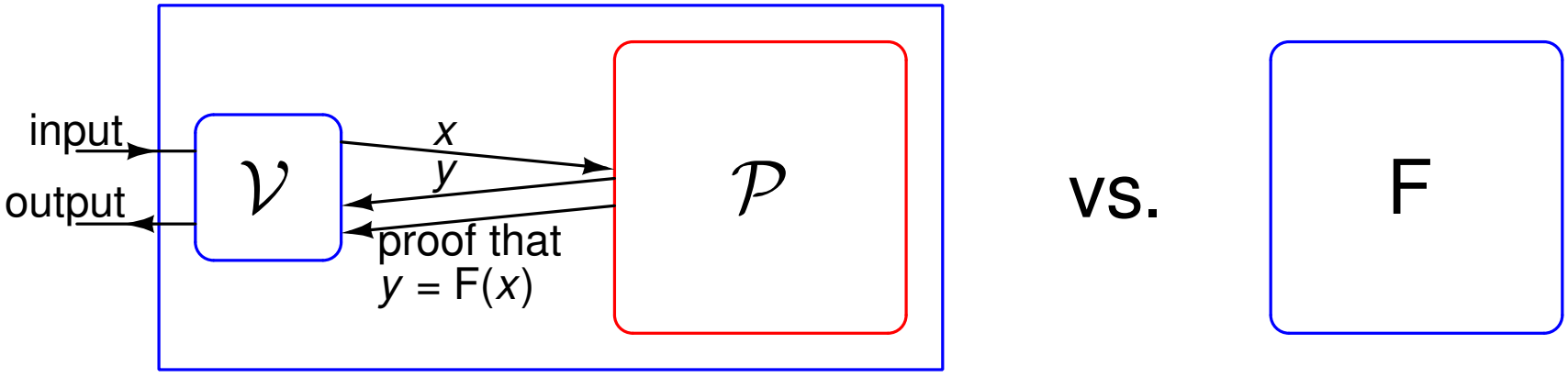

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350 nm: 1997 (Pentium II)
7 nm: $\approx$ 2017 [TSMC]
$\approx$ 20 year gap between
trusted and untrusted fab

Constraints: trusted fab = 350 nm; untrusted fab = 7 nm
200 mm^2 max chip area; 150 W max total power

Application #1: number theoretic transform

NTT: a Fourier transform over $\mathbb{F}_p$

Widely used, e.g., in computer algebra

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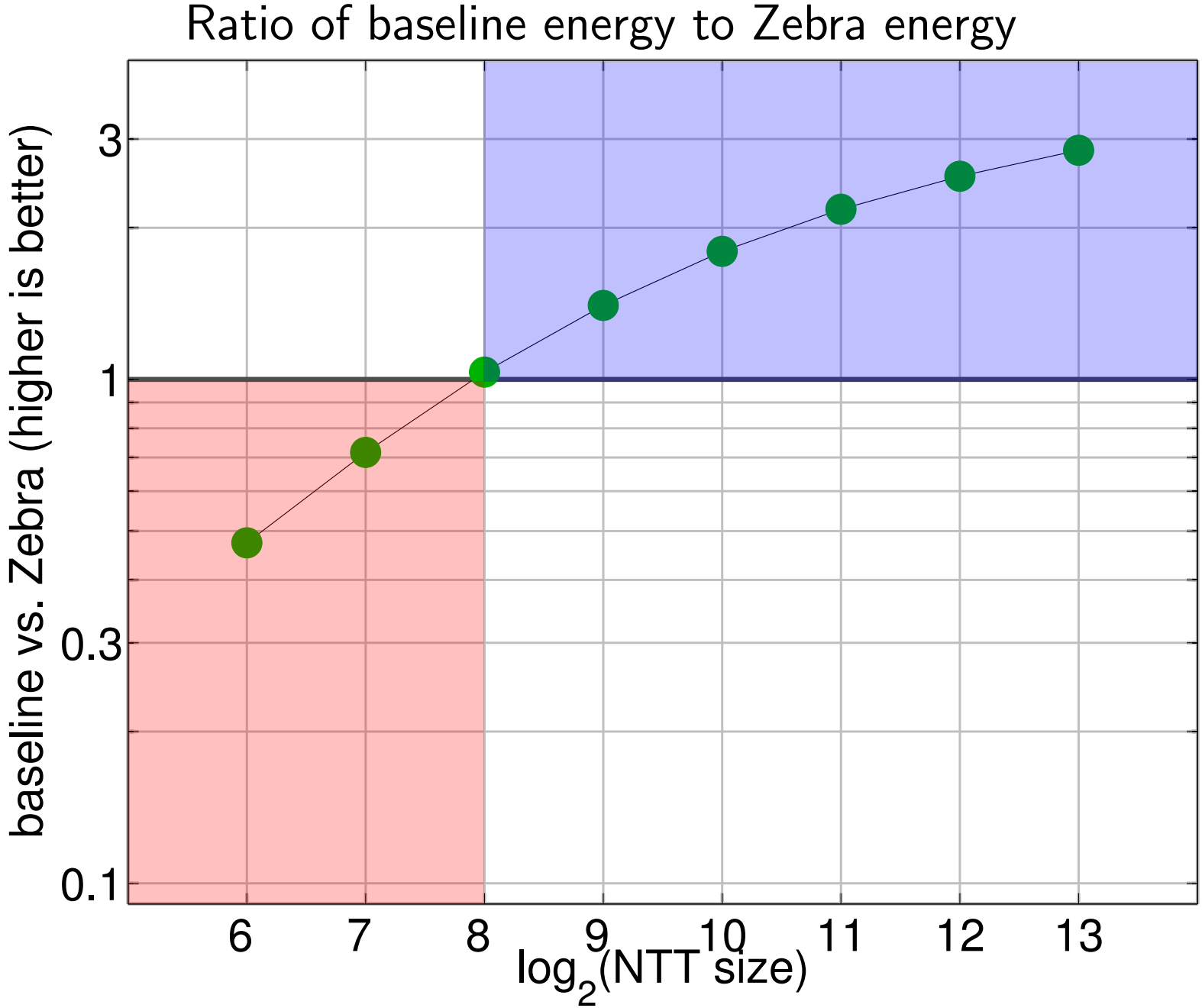

Application #2: Curve25519 point multiplication

Curve25519: a commonly-used elliptic curve

Point multiplication: primitive, e.g., for ECDH

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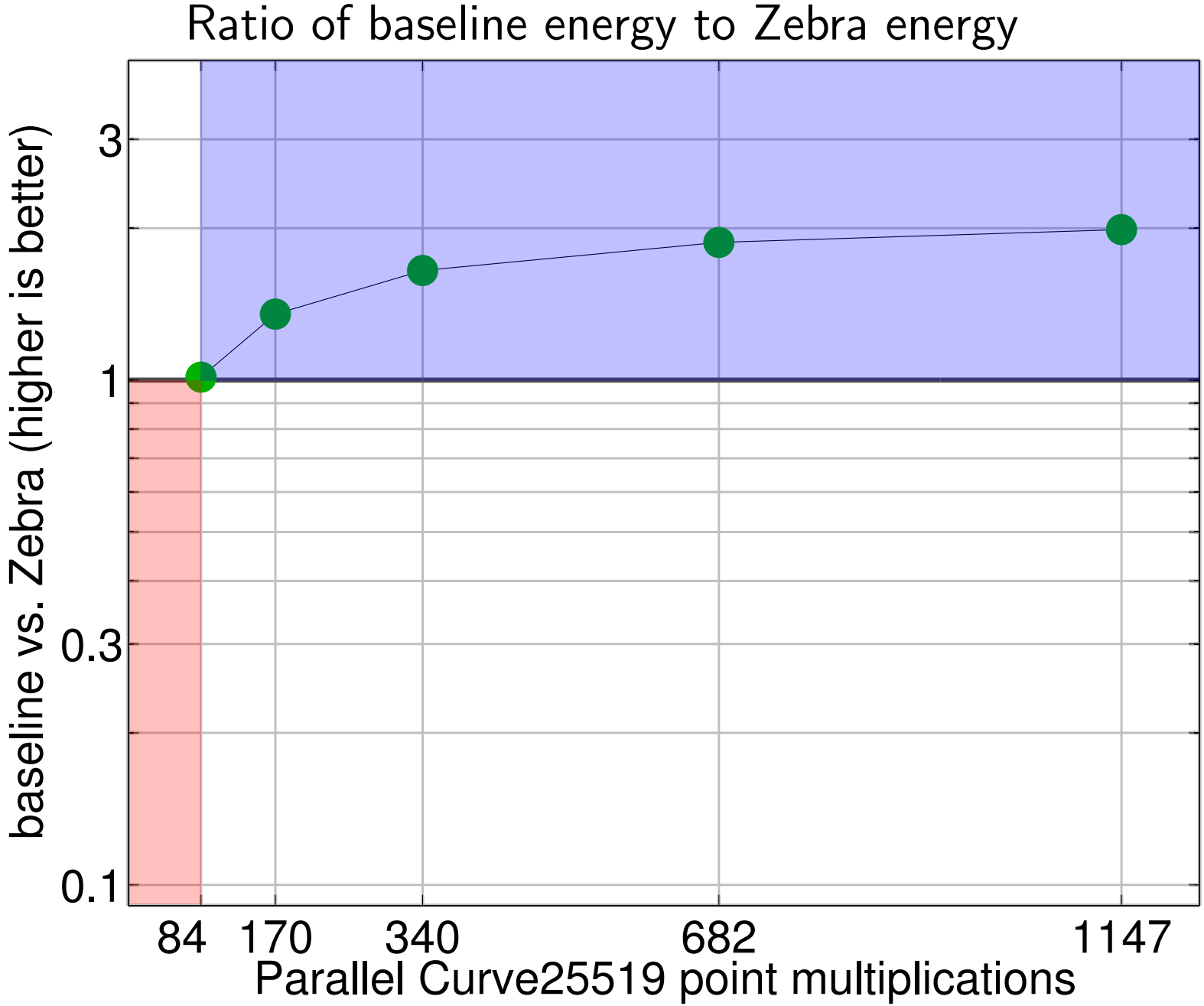

A **qualified** success

Zebra: a hardware design that saves costs...

...**sometimes**.

Summary of Zebra's applicability

1. Computation F must have a layered, shallow, deterministic AC
2. Must have a wide gap between cutting-edge fab (for $\mathcal{P}$) and trusted fab (for $\mathcal{V}$)
3. Amortizes precomputations over many instances
4. Computation F must be very large for $\mathcal{V}$ to save work
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Arguments versus IPs, redux

Design principle	**IPs** [GKR08, CMT12, VSBW13]	**Arguments** [GGPR13, SBVBPW13, PGHR13, BCTV14]
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Exploit locality	✓	
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Argument protocols seem friendly to hardware?

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. . . but we hope these issues are surmountable!

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Common to essentially all built proof systems

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5. Computation F

System	Amortization regime	Advice
Zebra	many $\mathcal{V}$-$\mathcal{P}$ pairs	short
Allspice [VSBW13]	batch of instances of a particular F	short
Bootstrapped SNARKs [BCTV14a, CTV15]	all computations	long
BCTV [BCTV14b]	all computations of the same length	long
Pinocchio [PGHR13]	all future instances of a particular F	long
Zaatar [SBVBPW13]	batch of instances of a particular F	long

Exception: [CMT12] with logspace-uniform ACs

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$\mathcal{V}$'s work: $6\text{ ms} + (|x| + |y|) \cdot 3\ \mu\text{s}$ on a 2.7 GHz CPU

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$\Rightarrow$ breaking even requires $>$ 1 CPU op per AC gate, e.g., computations over $\mathbb{F}_p$ rather than machine integers

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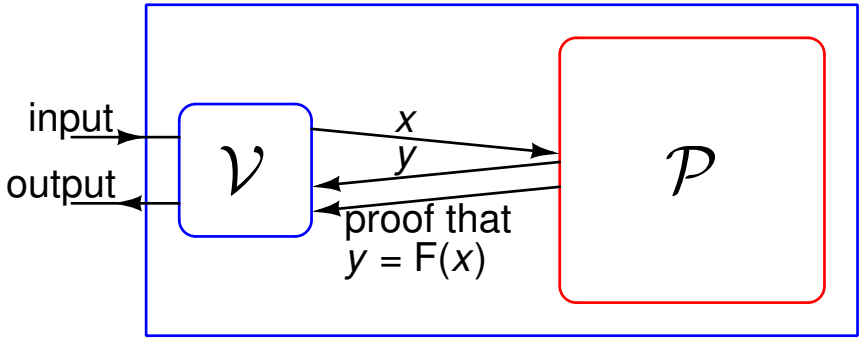
Recap



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+ First hardware design for a probabilistic proof protocol
+ Improves performance compared to trusted baseline

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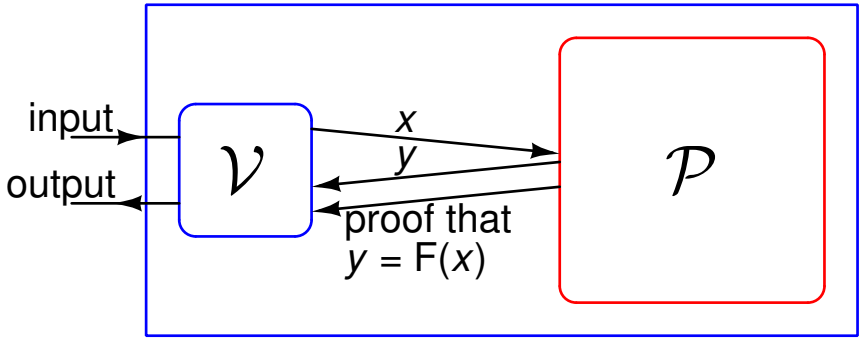

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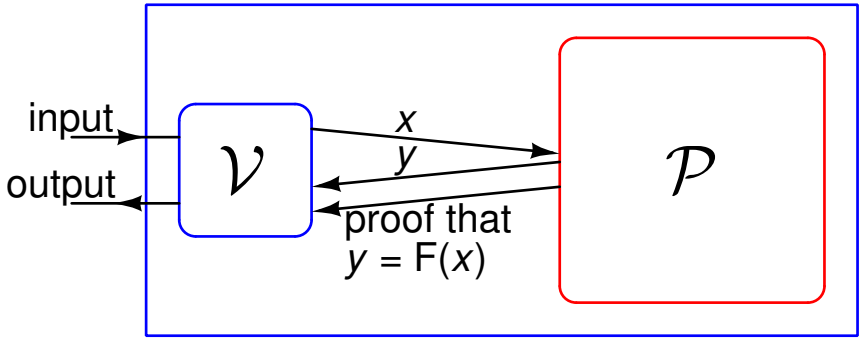
– Applicability is limited:

  precomputations must be amortized
  computation needs to be "big enough"
  large gap between trusted and untrusted technology
  does not apply to all computations

Recap



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Bottom line: Zebra is plausible—when it applies

`https://www.pepper-project.org/`